HEWLETT hp PACKARD

# TIME BASE GENERATOR INTERFACE KIT

model 12539A

OPERATING AND SERVICE MANUAL 20 AUG 1968

## SECTION I

## INTRODUCTION AND DESCRIPTION

### 1-1. INTRODUCTION.

1-2. Interface Kit 12539A generates real time intervals in decade steps from 100 microseconds to 1000 seconds (16.67 minutes) derived from a crystal oscillator. This card can be used as a source of timed interrupt for software clock. The kit consists of the following:

a. Interface Kit 12539A Time Base Generator Card, HP Part No. 02116-6119.

b. Time Base Generator Test.

1-3. Sections II through IV provide installation and programming, theory of operation and replaceable parts information for the Time Base Generator Card. Section V contains troubleshooting information. A supplement to this manual contains a description of the diagnostic program contained on the Time Base Generator Test-Binary Tape and the diagnostic listing.

### 1-4. DESCRIPTION.

1-5. The Time Base Generator Card contains command and interrupt logic, a 100 kHz oscillator, and eight decade frequency dividers. This card plugs into any of the interface card I/O slots of the Computer and assumes the lower Select Code of the slot.

1-6. SPECIFICATIONS.

Stability: 2 parts in $10^6$ per week.

Temperature Effects: 20 parts in $10^6$ over the temperature range of 15 to 35 C.

Total Stability: 1/2 second per 24-hour day.

## SECTION II

## INSTALLATION AND PROGRAMMING

### 2-1. INSTALLATION.

2-2. Open the Computer for access to the I/O cards and insert the Time Base Generator card in the desired I/O slot of the Computer. The slot connector transfers all signals to and from the Computer; no additional cabling is required. Close the Computer.

### 2-3. PROGRAMMING.

2-4. Table 2-1 provides a typical program example. This example is a subroutine which provides an execution delay of 8 milliseconds using the Time Base Generator. The "flag-test" (SFS) method is used, rather than interrupt.

Table 2-1. Program Example

```
DELAY   NOP
        LDA     .8      GET 8 FOR COUNTER
        CMA,    INA     MAKE NEGATIVE
        STA     COUNT   INITIALIZE COUNTER
        LDA     .1      GET CONTROL WORD FOR
        OTA     TBG     1 MILLISEC FLAGS & OUTPUT
LOOP    STC     TBG,C   START TIME BASE GEN.
        SFS     TBG     HAS PERIOD ELAPSED
        JMP     *-1     NO - CONTINUE TO WAIT
        ISZ     COUNT   1 PERIOD HAS ELAPSED
        JMP     LOOP    NOT THE LAST ONE, START ANOTHER
        JMP     DELAY,I TOTAL DELAY HAS ELAPSED, RETURN
*
TBG     EQU     nn      I/O ADDRESS OF TIME BASE GEN.
COUNT   NOP             LOCATION OF FLAG COUNTER
.8      DEC     8       FOR 8 FLAGS
.1      OCT     1       CONTROL WORD FOR 1 MILLISEC
```

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## SECTION III

## THEORY OF OPERATION

### 3-1. GENERAL THEORY OF OPERATION.

3-2. An Output from A (OTA) or an Output from B (OTB) instruction applies a 3-bit binary number to the Time Base Selection flip-flops, Bit 0, Bit 1, and Bit 2. This 3-bit number (IOBO0, IOBO1, and IOBO2) determines the time interval between interrupt (or SKF) signals to the Computer and are the three least significant bits of the A- or B-Register. When a different time interval is desired, the 3-bit number is changed (with another OTA/B instruction). For non-decade time intervals (e.g., 3 milliseconds), the nearest decade interrupt must be counted in software to form the desired interval. Table 3-1 lists the Computer outputs and the respective time intervals available from the card. Note that interrupt (or SKF) signals can be programmed to occur every $10^{n-1}$ milliseconds, where n is the 3-bit binary number from the A- or B-Register.

Table 3-1. Time Intervals

| I/O BUS OUTPUT (IOBO) | | | TIME INTERVAL |
|---|---|---|---|
| Bit 2 | Bit 1 | Bit 0 | |
| 0 | 0 | 0 | 0.1 Millisecond |
| 0 | 0 | 1 | 1 Millisecond |
| 0 | 1 | 0 | 10 Milliseconds |
| 0 | 1 | 1 | 0.1 Second |
| 1 | 0 | 0 | 1 Second |
| 1 | 0 | 1 | 10 Seconds |
| 1 | 1 | 0 | 100 Seconds |
| 1 | 1 | 1 | 1000 Seconds |

3-3. As a result of the OTA/B instruction, the IOO signal causes the Time Base Selection flip-flops and the eight decade dividers to be reset at time T3 to establish proper initial conditions. The IOBO signals cause the Time Base Selection flip-flops to set or remain reset, as applicable, and the flip-flop outputs provide enabling signals to the "and" gates on the outputs of the decade dividers. At this time, the output of the 100 kHz Oscillator is not enabled to the decade dividers since the Control flip-flop is still in a reset state.

3-4. A Set Control, Clear Flag (STC,CLF) instruction to the Time Base Generator Card initiates the time interval programmed by the OTA/B instruction. The STC portion of the instruction sets the Control flip-flop, which enables the Oscillator output to the decade dividers and resets the Error flip-flop. The Error flip-flop is set if the interrupt signal at the end of the programmed time interval is not acknowledged. The CLF portion of the instruction resets the Flag flip-flop so that it can be set to indicate the end of the selected time interval using the SFS instruction.

### 3-5. DETAILED THEORY OF OPERATION.

3-6. Figure 3-1 depicts the logic diagram for the Time Base Generator Card and Figure 3-2 depicts the location of parts on the board. Logic diagram reference designations preceded by MC are identified by part number in Section IV and the logic diagram for each Microcircuit package is shown in Figure 3-3.

3-7. TIME BASE SELECTION.

3-8. The outputs of the decade dividers are "anded" with the outputs of the Time Base Selection flip-flops. The output of the particular enabled "and" gate is combined with the true output of the Control flip-flops, and the true reset output of the Flag flip-flop to provide a true output from "and" gate MC87C. The output of MC87C is applied to the Flag Buffer flip-flop. The Flag Buffer flip-flop will not set until its input signal drops. This occurs when the applicable decade divider square-wave output drops, causing the output of gate MC87C to become false. After the Flag Buffer flip-flop is set, the Flag flip-flop sets on the arrival of the ENF signal at time T2 of the machine cycle. The interrupt or SKF signal (as applicable) is then initiated to the Computer, indicating the end of the selected time interval. (If the SKF method is to be used, a Skip on Flag Set (SFS) or a Skip on Flag Clear (SFC) instruction must be issued to test the condition of the Flag flip-flop.)

3-9. Assume a 3-bit (IOBO) input to the Time Base Selection flip-flops of 000. The true reset outputs of the flip-flops are applied to "and" gate MC45B. All other "and" gates contain at least one false input from the Time Base Selection flip-flops. When a STC instruction is issued, the Oscillator output is enabled to decade divider MC93. The square-wave output of MC93 becomes true and then returns to a false condition 0.1 millisecond after the STC instruction is issued. During the 0.1 millisecond interval, a true signal is applied to the Flag Buffer flip-flop. At the end of the interval, the Flag Buffer flip-flop sets and the interrupt and SKF circuits are initiated.

3-10. ERROR DETECTION.

3-11. The output of the particular enabled "and" gate on the output of the decade divider is combined with the set output of the Flag flip-flop at "and" gate MC123A. Therefore, the Error flip-flop is set if the Flag flip-flop is set. The Flag flip-flop will be set during the present time interval only when the previous time interval was not acknowledged by the Computer. (A Clear Flag (CLF) instruction must be issued after each time interval to permit recognition of the following time interval.) The condition of the Error flip-flop can be tested by a Load Into A (LIA) or a Load Into B (LIB) instruction. The IOI signal resulting from the LIA or LIB instruction enables "and" gate MC107A to provide a true IOBI4 signal to the A- or B-Register of the Computer. Therefore, if bit 4 of the applicable Register is true, at least one time interval was missed. The Error flip-flop is reset again by a CLF, STC instruction.

3-12. At completion of the use of the Time Base Generator card, a Clear Control (CLC) instruction should be programmed to reset the Control flip-flop and all decade dividers.

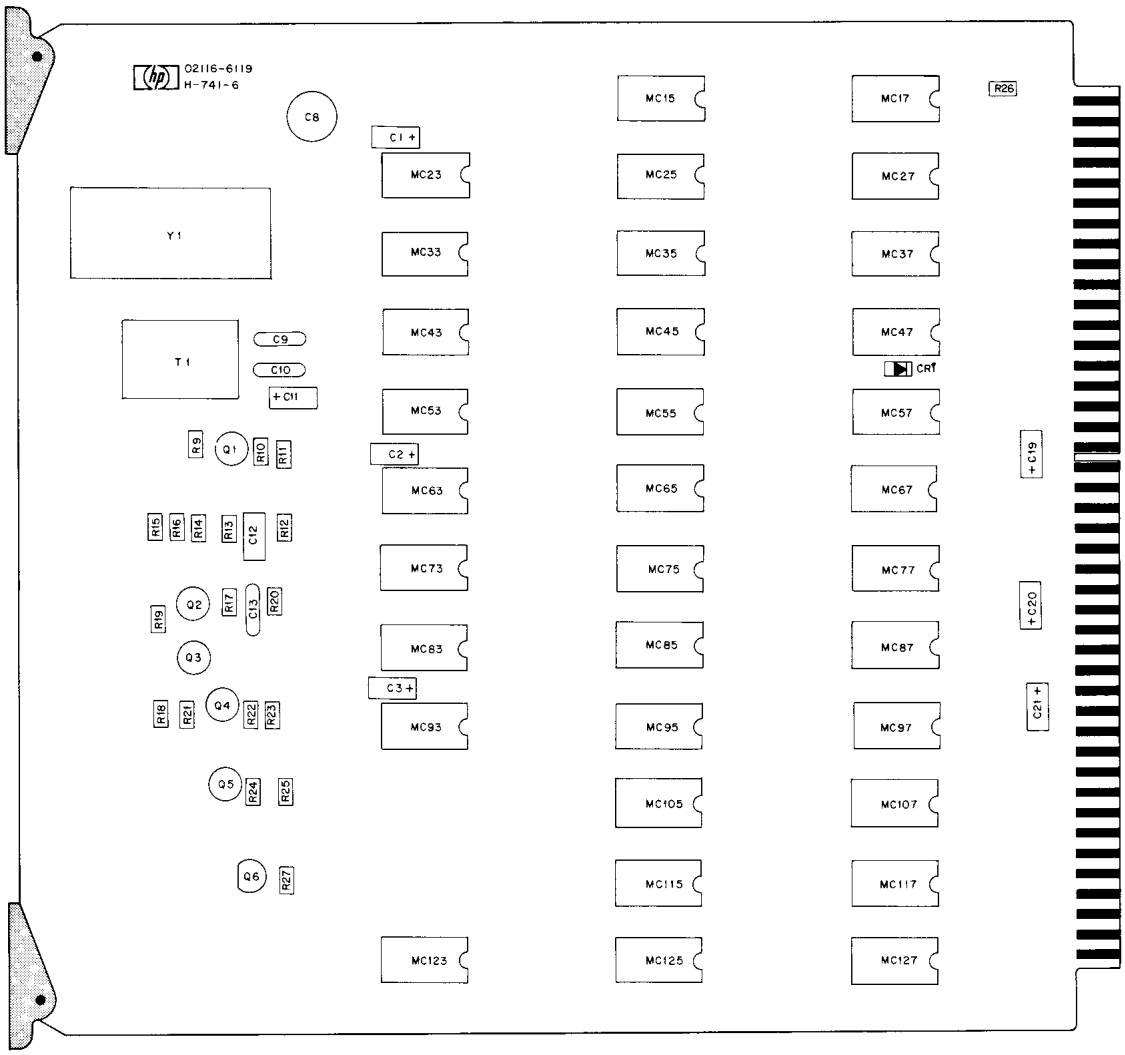


Figure 3-2. Time Base Generator, Parts Location Diagram

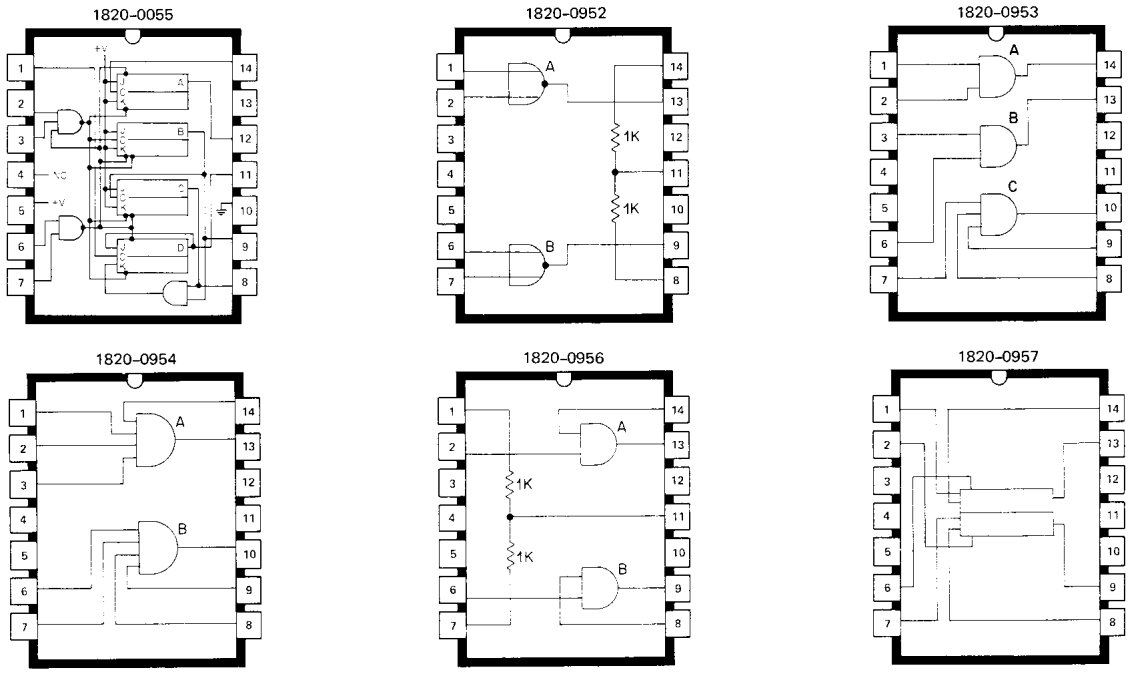


Figure 3-3. Microcircuit Packages, Top View

## SECTION IV

## REPLACEABLE PARTS

### 4-1. INTRODUCTION.

4-2. This section contains information for ordering replacement parts for the Time Base Generator Card. Refer to Table 4-1 for a list of replaceable parts in alpha-numerical order of their reference designations, with a description and HP part number for each part.

### 4-3. ORDERING INFORMATION.

4-4. To order a replacement part, address the order or inquiry to your local Hewlett-Packard field office. See the list at the back of this manual for field office addresses.

4-5. Specify the following information for each part when ordering:

a. Hewlett-Packard part number
b. Circuit reference designation
c. Description

4-6. To order a part not listed in Table 4-1, give a complete description of the part and include its function and location.

Table 4-1. Replaceable Parts for Time Base Generator Card

| REFERENCE DESIGNATION | DESCRIPTION | HP PART NO. | MFR CODE | MFR PART NO. |
|---|---|---|---|---|
| C1,2,3,11,19,20,21 | Capacitor, fixed, Tant, 1.0 uf ±10% | 0180-0291 | 56289 | 150D105X9035A2 |
| C8 | Capacitor, variable, 9 to 35 pf | 0121-0046 | 72982 | 538-011-E2PO-94R |
| C9 Factory | Capacitor, fixed, mica, 27 pf ±5% | 0160-2101 | 72136 | RDM15E270G3C |
| C9 adjusted | Capacitor, fixed, mica, 24 pf ±5% | 0160-0196 | 04062 | RDM15C240J3S |
| C9 value | Capacitor, fixed, mica, 20 pf ±5% | 0140-0204 | 72136 | RDM15C200J3C |
| C10 | Capacitor, fixed, mica, 470 pf ±5% | 0140-0149 | 72136 | DM15F471J |
| C12 | Capacitor, fixed, Mylar, 0.001 uf ±10% | 0160-0153 | 56289 | 192P10292-PTS |
| C13 | Capacitor, fixed, mica, 220 pf ±5% | 0160-0134 | 72136 | DM15F221J (300V) |
| CR1 | Diode | 1910-0022 | 28480 | - |
| MC15,25,35,45,97 | Integrated Circuit | 1820-0954 | 28480 | - |
| MC17,107 | Integrated Circuit | 1820-0956 | 28480 | - |
| MC23,33,43,53,63, 73,83,93 | Integrated Circuit | 1820-0055 | 28480 | - |
| MC27,57,65,75,85, 95,115,127 | Integrated Circuit | 1820-0952 | 28480 | - |
| MC37,47,55,77,87, 105,117,123,125 | Integrated Circuit | 1820-0953 | 28480 | - |
| MC67 | Integrated Circuit | 1820-0957 | 28480 | - |
| Q1 | Transistor, Silicon, NPN (S6515) | 1854-0019 | 28480 | - |
| Q2 thru Q5 | Transistor, Silicon, NPN (2N3646) | 1854-0094 | 28480 | - |
| Q6 | Transistor, Silicon, PNP (2N3906) | 1853-0036 | 28480 | - |
| R9 | Resistor, fixed, 68K ±5%, 1/4W | 0683-6835 | 01121 | CB 6835 |
| R10,20 | Resistor, fixed, 10K ±5%, 1/4W | 0683-1035 | 01121 | CB 1035 |
| R11 | Resistor, fixed, 47 ohms ±5%, 1/4W | 0683-4705 | 01121 | CB 4705 |
| R12 | Resistor, fixed, 8.2K ±5%, 1/4W | 0683-8225 | 01121 | CB 8225 |
| R13 | Resistor, fixed, 2.2K ±5%, 1/4W | 0683-2225 | 01121 | CB 2225 |
| R14 | Resistor, fixed, 33K ±5%, 1/4W | 0683-3335 | 01121 | CB 3335 |
| R15 | Resistor, fixed, 3.9K ±5%, 1/4W | 0683-3925 | 01121 | CB 3925 |
| R16 | Resistor, fixed, 2.7K ±5%, 1/4W | 0683-2725 | 01121 | CB 2725 |
| R17 | Resistor, fixed, 150 ohms ±5%, 1/4W | 0683-1515 | 01121 | CB 1515 |
| R18 | Resistor, fixed, 1.8K ±5%, 1/4W | 0683-1825 | 01121 | CB 1825 |
| R19,21 | Resistor, fixed, 6.8K ±5%, 1/4W | 0683-6825 | 01121 | CB 6825 |
| R22 | Resistor, fixed, 4.7K ±5%, 1/4W | 0683-4725 | 01121 | CB 4725 |
| R23,25,26 | Resistor, fixed, 470 ohms ±5%, 1/4W | 0683-4715 | 01121 | CB 4715 |
| R24,27 | Resistor, fixed, 1K ±5%, 1/4W | 0683-1025 | 01121 | CB 1025 |
| T1 | Transformer | 5212A-9A | 28480 | - |
| Y1 | Crystal Oscillator, 100 kHz | 0410-0021 | 28480 | - |

## SECTION V

## TROUBLESHOOTING

### 5-1. DIAGNOSTIC TEST.

5-2. To confirm proper operation of the Time Base Generator option, use the Diagnostic Test tape furnished with the Interface Kit. The operating procedure and all pertinent information, including the program listing, is supplied in the Time Base Generator Diagnostic Test supplement (a supplement to this manual).

5-3. If the Diagnostic indicates a failure of the Time Base Generator, the following procedures may be used to check the basic timing signals.

5-4. OSCILLATOR TEST.

5-5. Testing of the 100 kHz Oscillator on the Time Base Generator Card is accomplished with the card plugged into a single connector extender which is plugged into the Computer. Turn Computer power on. The output of the oscillator is checked at test point TP1, Figure 3-1. If the oscillator is operating properly, a 100 kHz non-symmetrical square-wave should be observed. The same square-wave should be observed at test point TP2 after the Control flip-flop is set by an STC instruction.

5-6. Replacement of crystal Y1, capacitors C8 or C9 may require selection of C9 to give proper circuit operation. Adjustment of C8 should allow tuning 100 kHz ±0.5 Hz. The value of C9 should be as large as possible while tuning this range. If the value of C9 is small and the value of C8 is large, the temperature stability is poorer.

5-7. The negative portion of the waveshape (between R13 and C12) should be flattened. This indicates sufficient loop gain to saturate while rotating C8 through its entire range. This ensures enough loop gain to oscillate at low temperature. A frequency standard of adequate accuracy should be used for selecting C9 (accuracy 1/107, readout 7 significant digits).

5-8. DECADE DIVIDER TEST.

5-9. To facilitate testing of the eight decade dividers (MC23, MC33, MC43, MC53, MC63, MC73, MC83, and MC93), the Time Base Generator Card is designed to accept a jumper (W2) between the output of MC93 and the input to MC53. With this jumper installed use an oscilloscope for testing. Before testing the decade dividers, the W2 jumper may be installed to cause reduction of the time interval for the last group of four decade dividers to one second. To enable the 100 kHz Oscillator output to the dividers, the Control flip-flop must be set by an STC instruction. At completion of testing, the W2 jumper must be removed if the card is to function properly.

HEWLETT hp PACKARD

# OPERATING AND SERVICE MANUAL

# 12539B

## TIME BASE GENERATOR INTERFACE KIT

(FOR 2100, 2114, 2115, AND 2116 COMPUTERS)

Card Assembly
12539-60001, Rev 1028, 1147

Note

This manual should be retained with the applicable computer system documentation.

12539-90002

HEWLETT-PACKARD COMPANY
11000 WOLFE ROAD, CUPERTINO, CALIFORNIA, U.S.A.

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# SECTION I

# GENERAL INFORMATION

## 1-1. INTRODUCTION.

1-2. This manual provides general information, installation and programming instructions, theory of operation, maintenance instructions, and replaceable parts information for the Hewlett-Packard 12539B Time Base Generator Interface Kit (figure 1-1).

## 1-3. DESCRIPTION.

1-4. GENERAL.

1-5. The 12539B Time Base Generator measures real-time intervals in decade steps from 0.1 millisecond to 1000 seconds (16.67 minutes). A 3-bit control word transferred to the time base generator by programmed instruction selects the time interval to be measured. The 100-kHz crystal-controlled oscillator used as the frequency standard for the time base generator allows generation of timing signals accurate to within 1/2 second per 24-hour day.

1-6. KIT CONTENTS.

1-7. The time base generator interface kit consists of a time base generator printed-circuit card (part no. 12539-60001) and the operating and service manual (part no. 12539-90002).

1-8. IDENTIFICATION.

1-9. This operating and service manual is identified on the title page by interface kit designation and nomenclature, card assembly part number and revision code, manual part number, and publication date. Refer to the information presented in the following paragraphs and ensure that this manual applies to the equipment being serviced.

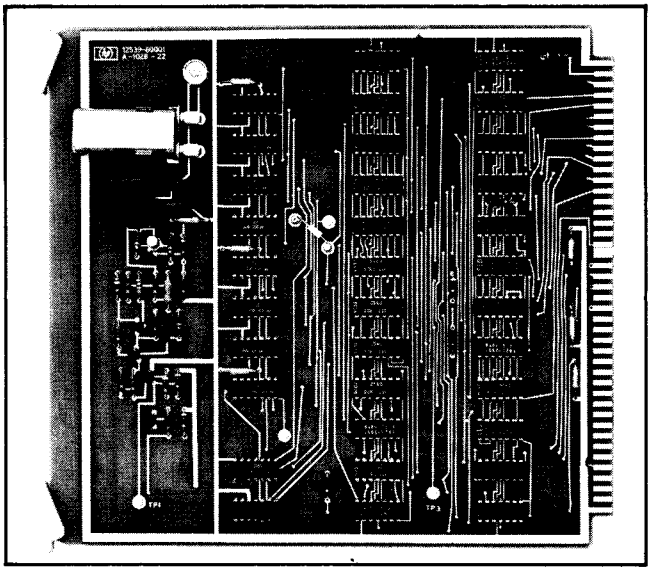


Figure 1-1. HP 12539B Time Base Generator Interface Kit

1-10. Hewlett-Packard uses five digits and a letter (00000A) for standard interface kit designation. If the designation of your kit does not agree with that on the title page of this manual, there are differences between your kit and the kit described in this manual. The appropriate manual or manual supplement is avilable at the nearest HP Sales and Service Office listed at the back of this manual.

1-11. Printed-circuit cards used as plug-in card assemblies or fixed wired assemblies are identified by a letter, a revision code, and a division code stamped on the card (e.g., A-1028-22). The letter identifies the version of the etched trace pattern on the unloaded card. The revision code (four middle digits) refers to the electrical characteristics of the loaded card. The division code (last two digits) identifies the Hewlett-Packard division which manufactured the card. If the revision code on the printed-circuit card does not agree with the revision code shown on the title page of this manual, there are differences between your card and the card described in this manual. These differences are described in manual supplements available at the nearest HP Sales and Service Office.

## 1-12. SPECIFICATIONS.

1-13. Table 1-1 lists the specifications for the HP 12539B Time Base Generator Interface Kit.

Table 1-1. Time Base Generator Specifications

| CHARACTERISTICS | SPECIFICATIONS |
|---|---|
| Time Base Intervals: | 0.1 millisecond<br>1 millisecond<br>10 milliseconds<br>100 milliseconds<br>1 second<br>10 seconds<br>100 seconds<br>1000 seconds |
| Time Base Accuracy: | 1/2 second per 24-hour day |
| Current Requirements from Computer Power Supply:<br>+12V<br>-12V<br>-2V<br>+4.5V | <br>0.01A<br>not used<br>0.42A<br>1.10A |

# SECTION II

# INSTALLATION AND PROGRAMMING

## 2-1. INTRODUCTION.

2-2. This section provides information for unpacking and inspection, reshipment, installation, and programming the HP 12539B Time Base Generator Interface Kit.

## 2-3. UNPACKING AND INSPECTION.

2-4. If the shipping carton is damaged upon receipt, request that the carrier's agent be present when the card is unpacked. Inspect the card for damage (cracks, broken components, etc.). If the card is damaged and fails to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing material for the carrier's inspection. The HP Sales and Service Office will arrange for repair or replacement of the damaged card without waiting for claims against the carrier to be settled.

## 2-5. RESHIPMENT.

2-6. If an item of the kit is to be shipped to Hewlett-Packard for service or repair, attach a tag to the item identifying the owner and indicating the service or repair to be accomplished. Include the model number of the kit.

2-7. Pack the item in the original factory packing material if available. If the original material is not available, standard factory packing material can be obtained from the nearest Hewlett-Packard Sales and Service Office.

2-8. If standard packing material is not used, wrap the item in Air Cap TH-240 cushioning (manufactured by Sealed Air Corporation, Hawthorn, N.J.) or equivalent and place in a corrugated carton (200 pound test material). Seal the shipping carton securely and mark it "FRAGILE" to ensure careful handling.

Note

In any correspondence, identify the kit by number. Refer any questions to the nearest Hewlett-Packard Sales and Service Office.

## 2-9. INSTALLATION.

2-10. The time base generator card obtains its operating currents from the computer power supply. Before installing the card, determine the current requirements of this card in combination with all other interface or accessory kits already installed in the computer. The computer system documentation defines the currents available from the computer and describes the procedures for calculating the total power supply current requirements. If the total current requirements exceed the limitations of the computer power supply, a Hewlett-Packard power supply extender unit or input/output extender unit must be used. See table 1-1 for the current requirements of the time base generator card.

2-11. After ensuring sufficient power, install the time base generator card as follows:

a. Turn power off at the computer.

b. Insert the time base generator card in the computer I/O slot corresponding to the desired select code.

c. Turn on power and perform the diagnostic test procedure, part no. 12539-90011, in the Manual of Diagnostics to verify proper operation of the time base generator card.

## 2-12. PROGRAMMING.

2-13. CONTROL WORD.

2-14. The desired time interval to be measured by the time base generator is selected by transferring a 3-bit control word from the computer A- or B-register to the time base generator. Table 2-1 lists the possible control word bit combinations and the time interval selected by each. Note that the time intervals are selected in increments equal to $10^{n-1}$ milliseconds where n is the decimal equivalent of the 3-bit control word. For non-decade time intervals (three milliseconds for example) a decade interval (in this case 1 millisecond) must be counted by software to form the desired interval.

Table 2-1. Control Word Combinations and Time Intervals

| CONTROL WORD | | | SELECTED TIME INTERVAL |
|---|---|---|---|
| Bit 2 | Bit 1 | Bit 0 | |
| 0 | 0 | 0 | 0.1 millisecond |
| 0 | 0 | 1 | 1 millisecond |
| 0 | 1 | 0 | 10 milliseconds |
| 0 | 1 | 1 | 100 milliseconds |
| 1 | 0 | 0 | 1 second |
| 1 | 0 | 1 | 10 seconds |
| 1 | 1 | 0 | 100 seconds |
| 1 | 1 | 1 | 1000 seconds |

NOTE: Bits 3 through 15 not used.

2-15. ERROR CHECK.

2-16. When more than one decade time interval is required for any given timing operation, the time base generator provides a means of ensuring that all selected intervals have been acknowledged by the computer. A status word, transferred from the time base generator to the computer A- or B-register by an LIA or LIB instruction, contains a single significant bit (bit 4). If this bit is a logic one, at least one time interval has been lost. This status word should be checked by software after each decade time interval.

2-17. SAMPLE PROGRAM.

2-18. Table 2-2 is a sample program demonstrating the operation of the time base generator. Under control of this program, the time base generator will provide a measured time interval of five seconds. This is done by counting five one second intervals with a software counter. After each one second interval, the error status bit is checked to ensure that all of the one second intervals are acknowledged by the computer.

2-19. The sample program is an actual program listing prepared on an HP computer system using the HP assembler software package.

Table 2-2. Sample Program

```
0001                ASMB,A,B,L,T
0002*
0003*  THIS IS A SAMPLE PROGRAM TO DEMONSTRATE THE OPERATION OF THE
0004*  TIME BASE GENERATOR.  UNDER CONTROL OF THIS PROGRAM, THE TIME
0005*  BASE GENERATOR WILL PROVIDE A MEASURED INTERVAL OF FIVE SECONDS.
0006*  THIS REQUIRES THAT FIVE DECADE INTERVALS OF ONE SECOND EACH
0007*  BE MEASURED AND COUNTED BY SOFTWARE.  AFTER EACH DECADE INTERVAL
0008*  IS MEASURED, THE ERROR STATUS IS CHECKED AND IF AN ERROR IS
0009*  DETECTED, THE COMPUTER HALTS WITH A T-REGISTER DISPLAY OF
0010*  102066 OCTAL.
0011*
0012  00100                 ORG 100B
0013*
0014  00100 000000  START NOP
0015  00101 060121        LDA .5      INITIALIZE COUNTER TO COUNT
0016  00102 070122        STA COUNT   FIVE DECADE INTERVALS.
0017*
0018*  THIS PART OF THE PROGRAM OPERATES THE TIME BASE GENERATOR.
0019*
0020  00103 060123        LDA CW      GET CONTROL WORD AND TRANSFER
0021  00104 102615        OTA TBG     TO TIME BASE GENERATOR.
0022  00105 102715        STC TBG     START TIME BASE GENERATOR
0023  00106 103115  GO    CLF TBG     ENABLE FLAG LOGIC.
0024  00107 102315        SFS TBG     HAS DECADE INTERVAL ELAPSED?
0025  00110 024107        JMP *-1     NO.  WAIT.
0026  00111 024112        JMP STAT    YES.  CHECK ERROR STATUS.
0027*
0028*  THIS PART OF THE PROGRAM CHECKS ERROR STATUS AND INCREMENTS
0029*  THE DECADE INTERVAL COUNTER.
0030*
0031  00112 102515  STAT  LIA TBG     GET STATUS WORD FROM TIME BASE
0032*                                    GENERATOR
0033  00113 050124        CPA ERR     DOES STATUS WORD INDICATE AN ERROR?
0034  00114 102066        HLT 66B     YES.  HALT COMPUTER.
0035  00115 034122        ISZ COUNT   NO.  INCREMENT COUNTER.  IS TIME
0036*                                    INTERVAL COMPLETE?
0037  00116 024106        JMP GO      NO.  START ANOTHER DECADE INTERVAL.
0038  00117 106715        CLC TBG     YES.  STOP DECADE COUNTERS.
0039  00120 102077        HLT 77B     HALT COMPUTER.
0040*
0041*  CONSTANT AND STORAGE INFORMATION.
0042*
0043  00121 177773  .5    DEC -5
0044  00122 000000  COUNT BSS 1
0045  00123 000004  CW    OCT 4
0046  00124 000020  ERR   OCT 20
0047  00015         TBG   EQU 15B
0048*
0049                      END START
**  NO ERRORS*
```

# SECTION III

# THEORY OF OPERATION

## 3-1. INTRODUCTION.

3-2. This section provides functional and detailed theory of operation for the 12539B Time Base Generator Interface Kit.

## 3-3. FUNCTIONAL THEORY OF OPERATION.

3-4. Figure 3-1 is a block diagram of the time base generator card and a flow chart showing the functional operation of the time base generator card. The program instructions shown in the flow chart are the same as those used in the sample program in table 2-2 in section II of this manual.

3-5. Operation of the time base generator begins with the transfer of a 3-bit control word from the computer A- or B-register to the Time Base Selection Register with an OTA or OTB instruction. The next instruction (STC,C) sets the Control FF and clears the Flag and Flag Buffer FFs. The set-side output of the Control FF gates the shaped 100-kHz signal to the decade divider circuits. This marks the beginning of the time interval. The set-side output of the Control FF and the clear-side output of the Flag FF enable the Time Flag Gate. An output from the Time Flag Gate signifies the end of the time interval as described in the following paragraphs.

3-6. The SFS instruction tests the state of the Flag FF. The Flag FF at the present time is in the clear state so the JMP *-1 instruction will be executed followed by the SFS instruction again. This wait-for-flag loop continues until the Flag FF is set.

3-7. At the end of the selected time interval, an output from the Time Flag Gate sets the Flag Buffer FF. The output of the Flag Buffer FF is gated with an ENF signal at the next computer time T2 which sets the Flag FF. The time base generator card then supplies an SKF signal which causes the computer to skip the JMP *-1 instruction and proceed with the program. The time spent in the wait-for-flag loop is that time selected by the control word that was initially transferred to the time base generator.

## 3-8. DETAILED THEORY OF OPERATION.

3-9. GENERAL.

3-10. Refer to the time base generator logic diagram, figure 4-2, in section IV of this manual while reading the detailed theory of operation discussion.

3-11. For an index of signals on the 86-pin edge of the time base generator card, refer to the computer system documentation.

3-12. All logic levels on the time base generator card are positive-true. The term "true" refers to a level of approximately +3.5V and "false" refers to approximately ground level. These signal levels vary somewhat depending on the integrated circuit package involved. Detailed signal level information for the various integrated circuit packages used on time base generator card is provided in figure 4-1 in section IV of this manual.

3-13. POWER-ON LOGIC.

3-14. When power is initially applied to the computer or the computer PRESET switch is pressed, the computer supplies a POPIO and a CRS signal to the time base generator card. The POPIO signal sets the Flag Buffer FF and the CRS signal clears the Control FF. An ENF signal at the next computer time T2 is gated with the set-side output of the Flag Buffer FF to set the Flag FF. The true clear-side output of the Control FF is applied to the clear input of the decade dividers ensuring that they are all initially in the clear state. The false set-side output of the Control FF inhibits "and" gate MC125A to prevent the 100-kHz signal from clocking the decade dividers.

3-15. TIME STANDARD LOGIC.

3-16. The time standard logic consists of a 100-kHz crystal oscillator, a pulse shaping network, and eight decade dividers.

3-17. Transistor Q1 and associated components make up the 100-kHz oscillator. Crystal Y1 provides the frequency standard and capacitor C8 allows fine adjustment of the oscillator output frequency. Refer to section IV for oscillator adjustment procedures.

3-18. Transistors Q2 and Q3 form a Schmitt trigger circuit that shapes the output of the oscillator to a nonsymmetrical square wave for use by the integrated circuit decade dividers. Transistors Q4 and Q5 ensure that the level of the 100-kHz signal meets the input requirements of the decade dividers. "And" gate MC125A allows the control logic to control the application of the 100-kHz signal to the decade dividers as described in paragraph 3-27.

3-19. The shaped and gated 100-kHz signal is applied to the first of the eight decade dividers. The decade dividers are wired externally to operate as binary coded decimal counters with a count added each time the input signal (pin 14) swings negative. The output signal (pin 11) swings positive on the eighth count and negative on the tenth

count. The negative swing adds one count to the next divider stage. The output signals from each of the decade dividers are applied to their respective Time Base Selection Gates.

3-20. TIME BASE SELECTION LOGIC.

3-21. The time base selection logic consists of three Time Base Selection FFs and eight Time Base Selection Gates.

3-22. The desired time interval to be measured by the time base generator card is encoded into a 3-bit control word. This control word is transferred from the computer A- or B-register to the Time Base Selection FFs by an OTA or OTB instruction with the select code of the time base generator. Either of these instructions supply true SCM, SCL, IOG, and IOO signals and the 3-bit control word (IOBO 0, IOBO 1, and IOBO 2) to the time base generator.

3-23. The IOO signal is true during time T3T4. A T3 signal from the computer is gated by the IOO signal to clear the Time Base Selection FFs. When the T3 signal goes false, the 3-bit control word is loaded into the Time Base Selection FFs. The IOO signal also clears the eight decade dividers at time T3T4.

3-24. The output of the Time Base Selection FFs are connected to the eight Time Base Selection Gates so that only one of the gates will receive three true inputs from the FFs for any given control word. The fourth input to these gates is the output of the respective decade divider. In this manner, the time period specified by the 3-bit control word is selected by the time base selection logic.

3-25. CONTROL LOGIC.

3-26. After the control word has been loaded into the Time Base Selection FFs, the time base generator is ready to begin measuring the time period. An STC,C instruction with the select code of the time base generator marks the beginning of the time period. As a result of this instruction, the time base generator card receives true IOG, SCM, SCL, STC, and CLF signals from the computer.

3-27. The STC signal sets the Control FF. The true set-side output of the Control FF enables the 100-kHz signal to the decade dividers and provides one of the enabling signals to the Time Flag Gate (MC87C).

3-28. The CLF signal clears the Flag Buffer and Flag FFs. The true clear-side output of the Flag FF provides another enabling signal to the Time Flag Gate. The decade dividers are now counting the 100-kHz signal and continue to count until the selected time interval has elapsed.

3-29. FLAG LOGIC.

3-30. The flag logic monitors the output of the time Flag Gate for a signal indicating the end of the desired time period. The Time Flag Gate has two true inputs as described in paragraphs 3-27 and 3-28. The third input is taken from the Time Base Selection Gates.

3-31. For discussion purposes, assume that the Time Base Selection Gate MC25B has been enabled by the Time Base Selection FFs. When the decade dividers have counted for 0.8 second, the output of divider MC53 goes positive (paragraph 3-19). This positive signal is gated through MC25B and the Time Flag Gate to the clock input of the Flag Buffer FF. At the count of one second, the output of divider MC53 goes negative and sets the Flag Buffer FF. At the next computer time T2, an ENF signal is gated with the true set-side output of the Flag Buffer FF to set the Flag FF.

3-32. When the Flag FF is in the set state, the time base generator card generates an SRQ signal and, if programmed to do so, generates FLG and IRQ signals or an SKF signal. These signals indicate to the computer that the requested time interval has ended. The following paragraphs describe how these signals are generated and how they are used by the computer.

3-33. SKIP-ON-FLAG SIGNAL. If the computer is programmed to wait for the Flag FF to be set (SFS instruction followed by a JMP *-1 instruction for example), the resulting SFS signal gated with the set side of the Flag FF generates an SKF signal. This causes the computer to skip the next programmed instruction (JMP *-1) and proceed with the program. Figure 3-2 illustrates the generation of an SKF signal by the time base generator card. Notice that an SKF signal can also be generated when the Flag FF is in the clear state by programming a SFC instruction. Either way, the state of the Flag FF is being tested and the computer must be programmed to respond accordingly.

3-34. INTERRUPT SIGNALS. If the computer interrupt system has been enabled by an STF 00 instruction, the time base generator can be used to generate timed interrupts. Figure 3-3 illustrates the functions involved in an interrupt operation. To interrupt the main program at the end of a measured time interval, the following conditions must be met at the time base generator card:

a. Control FF set (paragraph 3-27).

b. Flag Buffer FF set (paragraph 3-31).

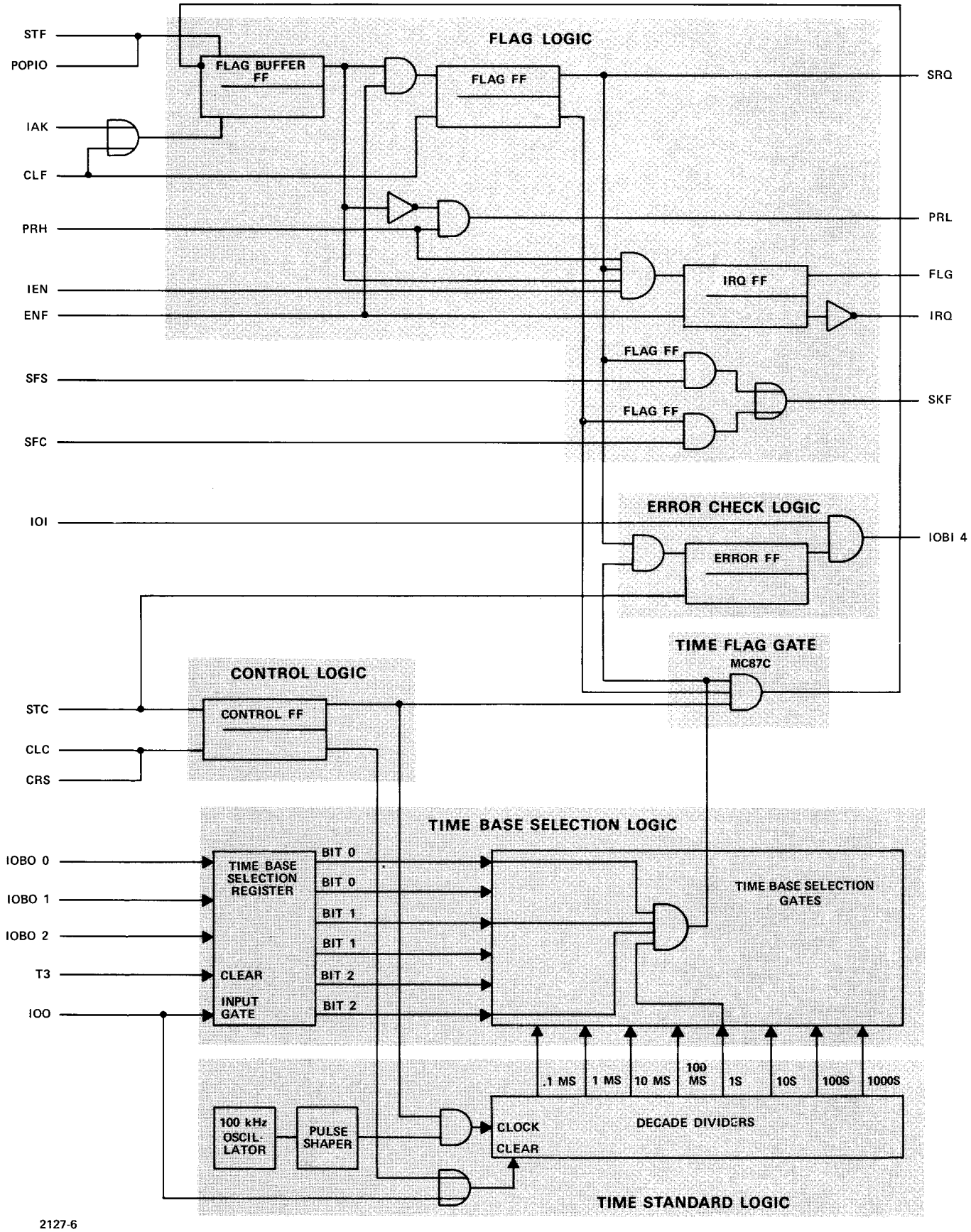
c. Flag FF set (paragraph 3-31).

d. IEN signal true (interrupt system enabled).

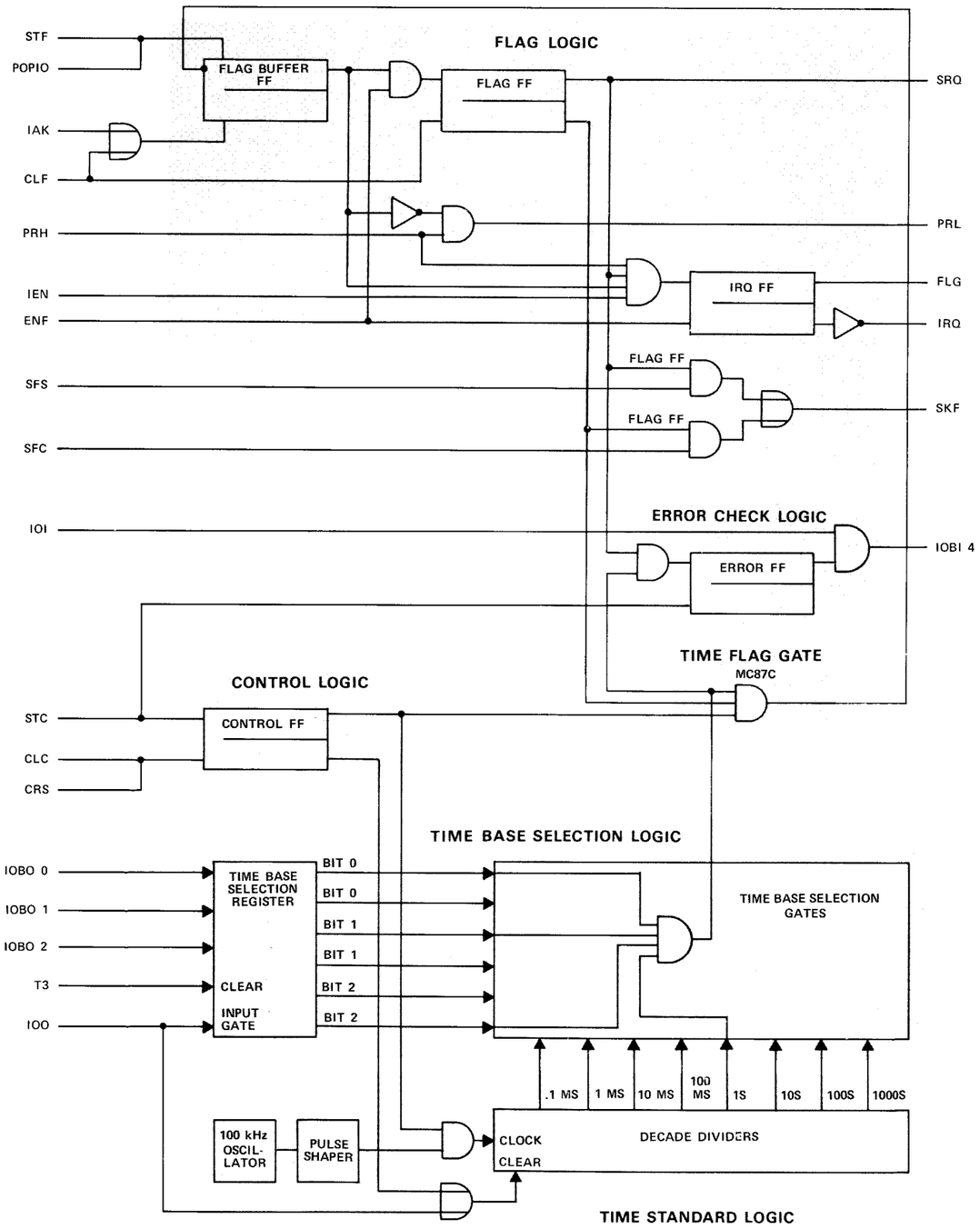
e. PRH signal true (no higher priority interrupts).

3-35. When all of these conditions are established, an SIR signal at time T5 sets the IRQ FF which generates true FLG and IRQ signals. These signals are used by the computer I/O control and addressing circuits to generate an interrupt signal.

3-36. At time T2 following the interrupt an ENF signal clears the IRQ FF. An SIR signal again sets the IRQ FF if the PRH signal is still true at time T5. The FLG and IRQ signals this time are used by the computer I/O control and addressing circuits to encode the interrupt address.


FLAG LOGIC
STF
POPIO
FLAG BUFFER FF
FLAG FF
SRQ
IAK
CLF
PRH
PRL
IEN
ENF
IRQ FF
FLG
IRQ
FLAG FF
SFS
SKF
FLAG FF
SFC
ERROR CHECK LOGIC
IOI
IOBI 4
ERROR FF
TIME FLAG GATE
MC87C
CONTROL LOGIC
STC
CONTROL FF
CLC
CRS
TIME BASE SELECTION LOGIC
IOBO 0
IOBO 1
IOBO 2
T3
IOO
TIME BASE SELECTION REGISTER
CLEAR
INPUT GATE
BIT 0
BIT 0
BIT 1
BIT 1
BIT 2
BIT 2
TIME BASE SELECTION GATES
.1 MS
1 MS
10 MS
100 MS
1S
10S
100S
1000S
100 kHz OSCIL-LATOR
PULSE SHAPER
CLOCK
CLEAR
DECADE DIVIDERS
TIME STANDARD LOGIC

2127-6



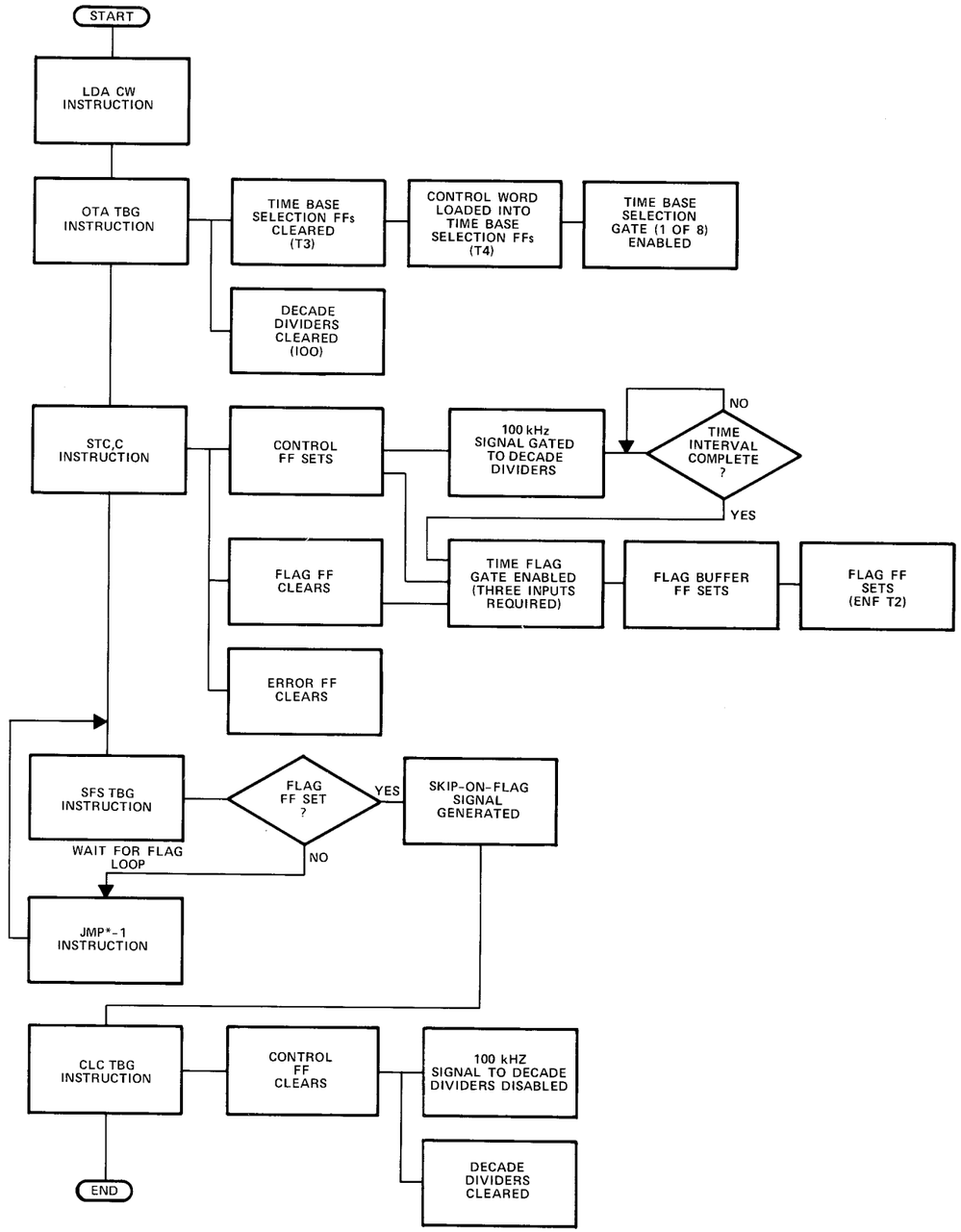




Figure 3-1. Time Base Generator Simplified Logic Diagram and Functional Operation Flow Chart

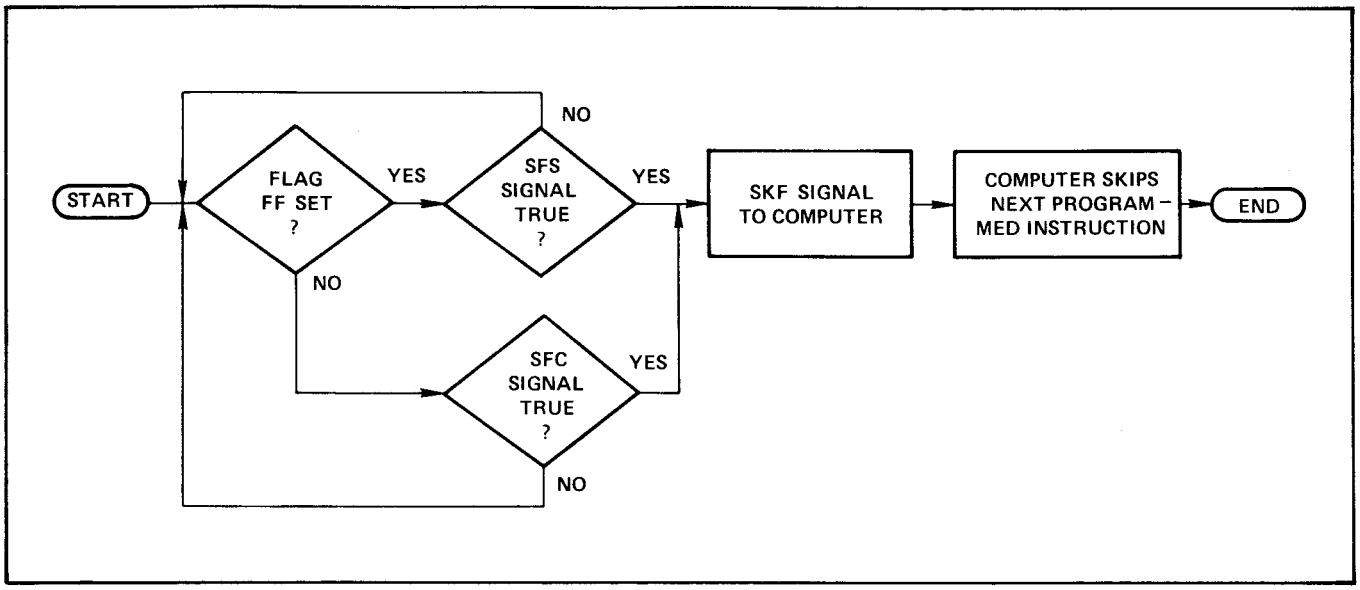



Figure 3-2. Skip-On-Flag Signal Generation Flow Chart

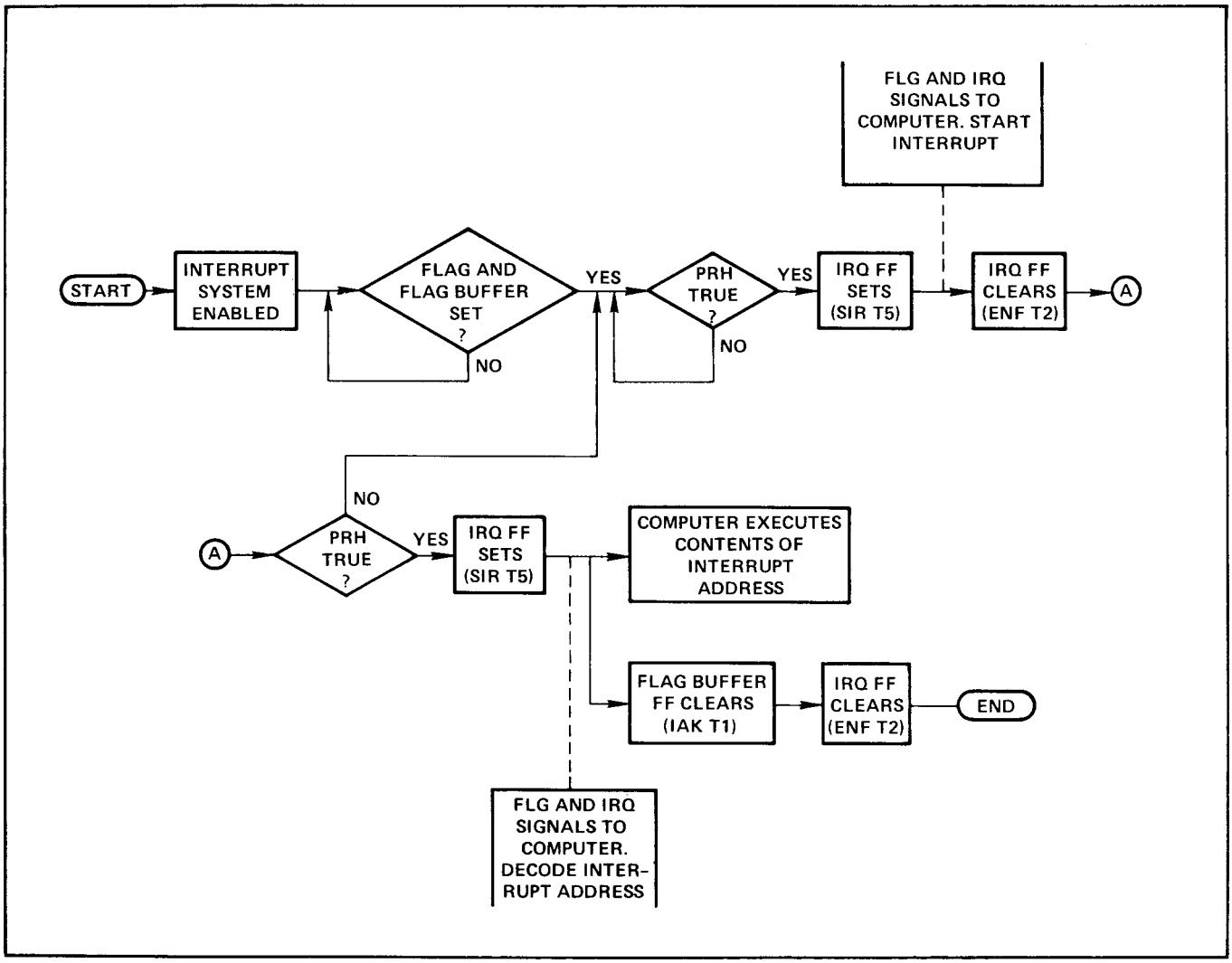



Figure 3-3. Interrupt Operation Flow Chart

3-37. The next machine cycle will be under control of the instruction located at the interrupt address in memory. During this machine cycle, an IAK signal at time T1 clears the Flag Buffer FF and an ENF signal at time T2 clears the IRQ FF. The Flag FF remains set to inhibit lower priority interrupts by providing a false PRL signal.

3-38. At this point, the computer normally enters an interrupt subroutine. A CLC instruction is required at the beginning of the subroutine to disable the decade dividers and prevent the Error FF (paragraph 3-42) from being set. Also, just before leaving the subroutine, a CLF instruction is required to enable lower priority interrupts.

3-39. SERVICE REQUEST SIGNAL. If the computer is equipped with the Direct Memory Access (DMA) accessory, and the DMA circuits have been initialized, the operation of the time base generator can be controlled by DMA. When the Flag FF is set, indicating the end of a measured time period, the time base generator supplies a true SRQ signal which enables the DMA circuits. The DMA circuits then suspend the computer program for one machine cycle, transfer a new 3-bit control word to the time base generator, and restart the time base generator.

3-40. Refer to the applicable DMA accessory operating and service manual for detailed information on DMA controlled operations.

3-41. ERROR CHECK LOGIC.

3-42. The Error FF monitors the set-side output of the Flag FF and the output of the Time Base Selection Gates. If the Flag FF is set, and the selected decade divider output is allowed to go positive a second time, the Error FF is set. This can occur during interrupt operations, for example, if an interrupt request is ignored by the computer. A set Error FF then indicates that at least one time period has been missed.

3-43. The state (set or cleared) of the Error FF is read onto the IOBI 4 line and loaded into the computer A- or B-register by an LIA or LIB instruction addressed to the time base generator. Bit 4 of the A- or B-register can then be checked by software for a possible error condition.

# SECTION IV

# MAINTENANCE

## 4-1. INTRODUCTION.

4-2. This section provides maintenance information for the HP 12539B Time Base Generator Interface Kit. Included are preventive maintenance instructions, troubleshooting instructions, and maintenance data consisting of integrated circuit pin connections and characteristics (figure 4-1), a time base generator printed-circuit card replaceable parts list (table 4-1), and a time base generator card parts location and logic diagram (figure 4-2).

## 4-3. PREVENTIVE MAINTENANCE.

4-4. Incorporate preventive maintenance for the time base generator with the preventive maintenance routines for the computer system. Inspect the time base generator card for cracked, broken, or burned components, insulation, and connections.

4-5. Check the oscillator output frequency at test point TP1 using a Hewlett-Packard 5244L Electronic Counter or equivalent. The frequency should be 100-kHz ±0.5 Hz. If the frequency is not within tolerance, adjust the frequency according to the oscillator adjustment procedures given in paragraph 4-10.

## 4-6. TROUBLESHOOTING.

4-7. Most malfunctions on the time base generator card can be traced by performing the diagnostic program procedure (part no. 12539-90008 for 2100A Computers or part no. 12539-90003 for 2114, 2115, and 2116 Computers) in the Manual of Diagnostics and analyzing error halts as they occur. Use the maintenance data contained in this section to isolate malfunctions to the component level.

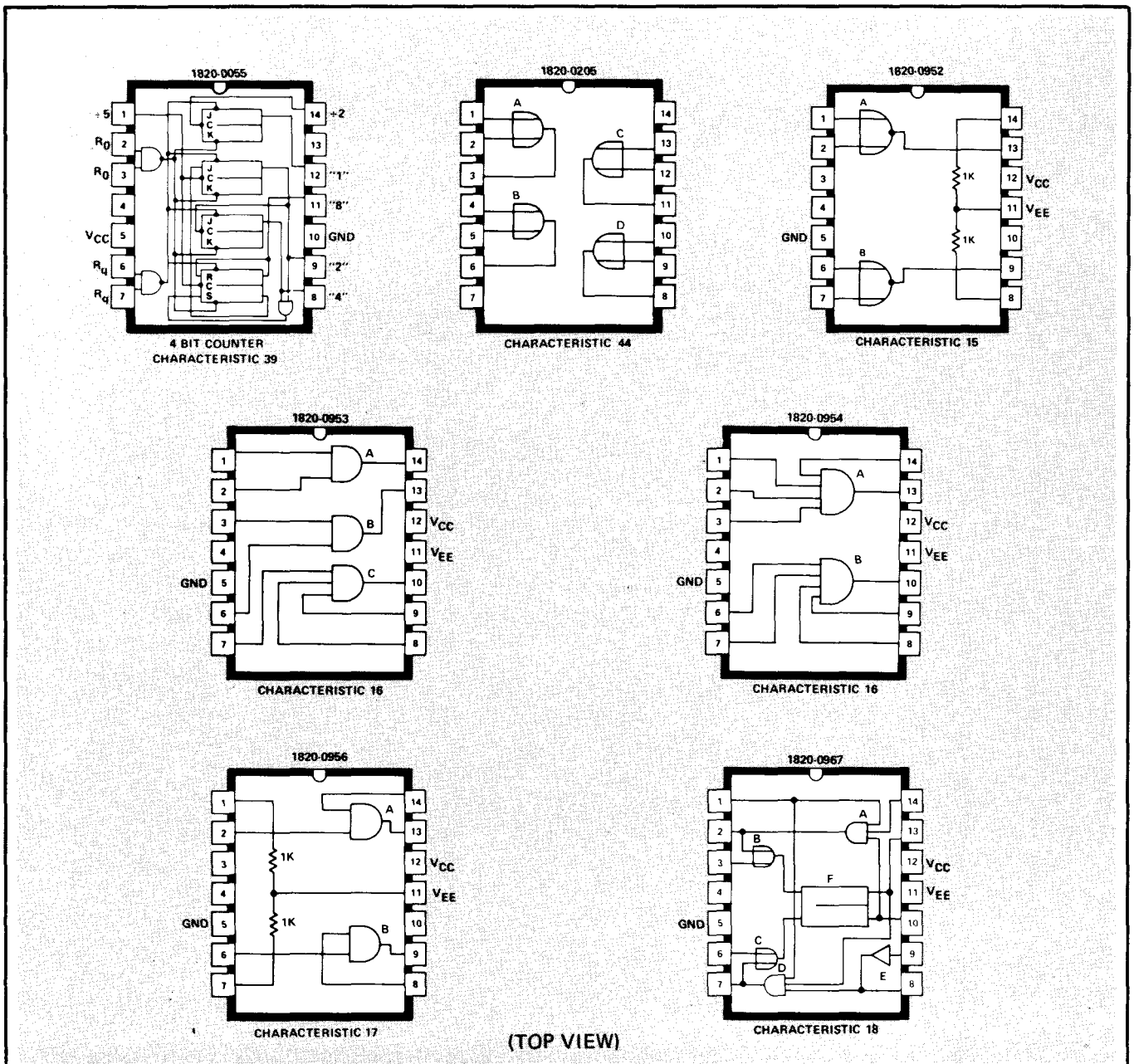
4-8. To facilitate testing the decade dividers, jumper W1 may be moved to position B. This reduces the time interval required to operate the last four divider circuits. With W1 in position B, decade dividers MC63, MC73, MC83, and MC93 will operate normally; however, decade divider outputs from MC23, MC33, MC43, and MC53 will occur at 1 second, 0.1 second, 10 millisecond, and 1 millisecond intervals respectively.

## 4-9. OSCILLATOR ADJUSTMENT.

4-10. Using a Hewlett-Packard 5244L Electronic Counter or equivalent frequency measuring device, observe the oscillator output frequency at test point TP1. Adjust capacitor C8 to obtain an output frequency of 100-kHz ±0.5 Hz.

Note

It may be necessary to replace capacitor C9 with a different value to achieve the correct output frequency. For maximum temperature stability, ensure that the replacement value for C9 be as large as possible while maintaining the required oscillator frequency.



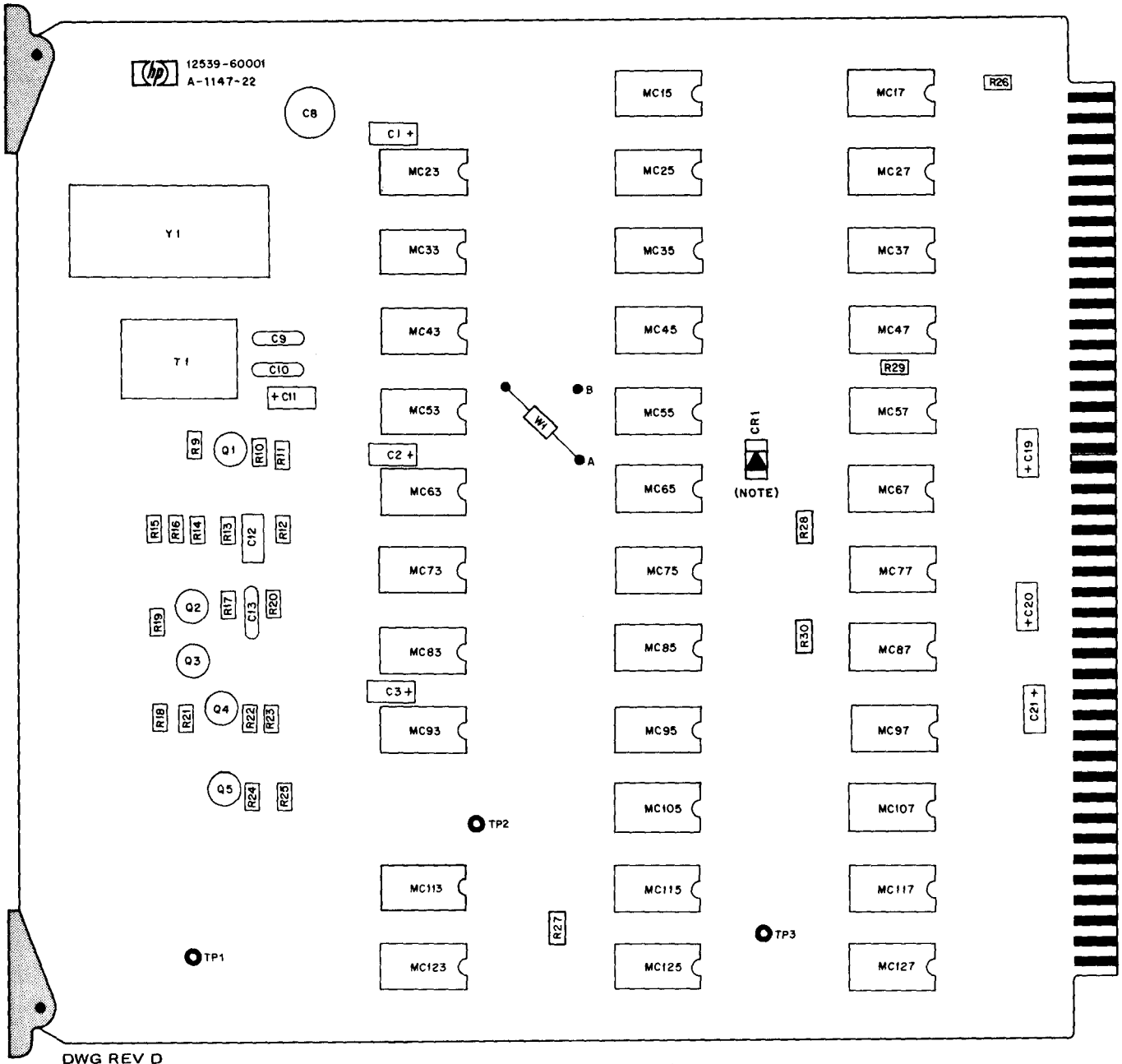

| CHARACTERISTIC | INPUT LEVEL | | OUTPUT LEVEL | | OPEN INPUT ACTS AS: | MAXIMUM PROPAGATION DELAY | |
|---|---|---|---|---|---|---|---|
| | LOGIC 1 (VOLTS, MIN) | LOGIC 0 (VOLTS, MAX) | LOGIC 1 (VOLTS, MIN) | LOGIC 0 (VOLTS, MAX) | | TO 1 (NANOSEC) | TO 0 (NANOSEC) |
| 15 | 1.25 | 0.5 | 2.35 | - 0.36 | 0 | 14 | 12 |
| 16 | 1.8 | 0.0 | 1.5 | 0.22 | 0 | 4.5 | 4 |
| 17 | 1.25 | 0.5 | 2.25 | - 0.36 | 0 | 18 | 18 |
| 18 | — | 0.5 | 2.35 | - 0.36 | 0 | 15 | 25 |
| 39 | 2.0 | 0.8 | 2.4 | 0.4 | — | 100 | 100 |
| 44 | 1.8 | 1.1 | 2.5 | 0.4 | 1 | 15 | 15 |

Figure 4-1. Integrated Circuit Pin Connections and Characteristics

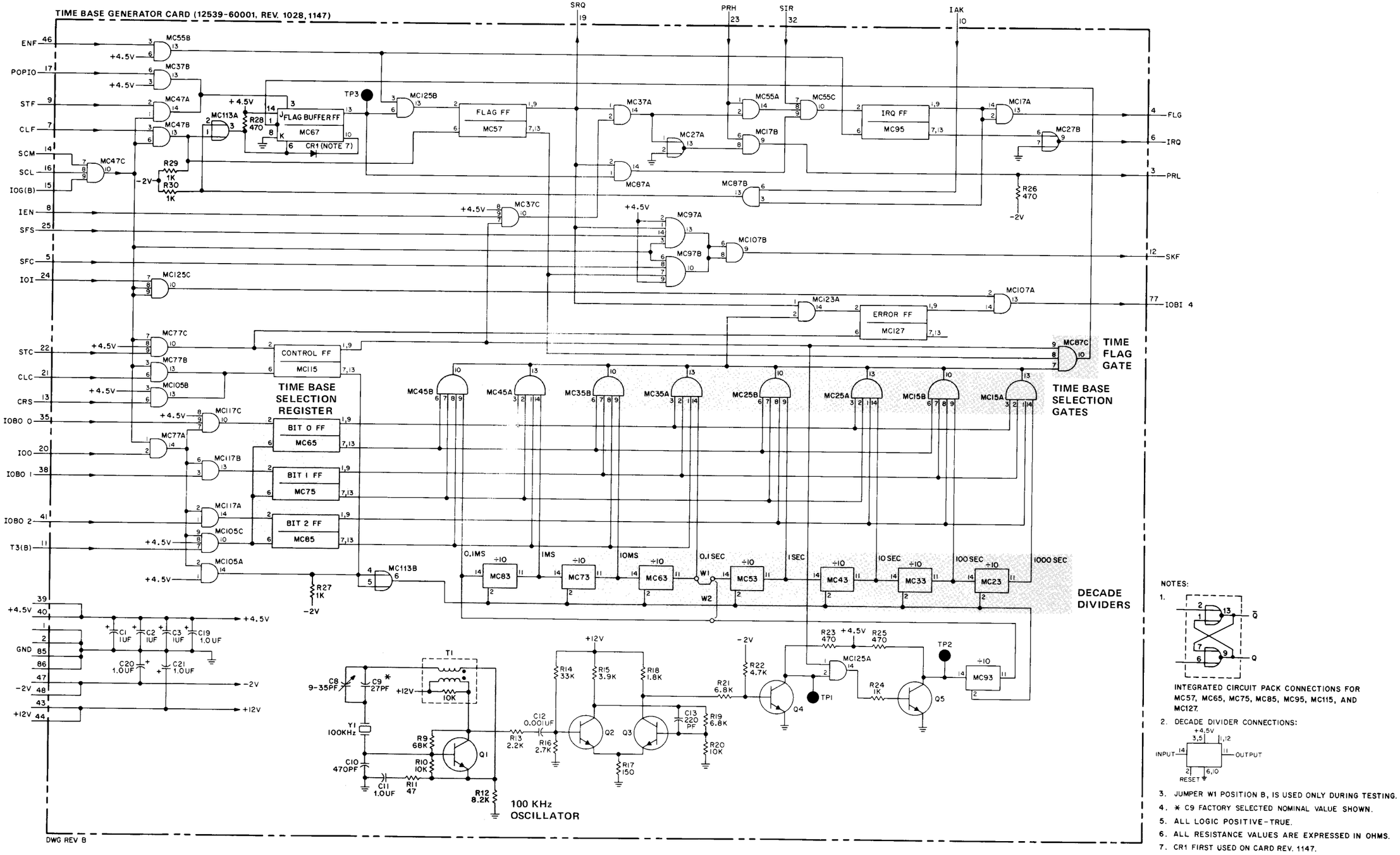
Table 4-1. Time Base Generator Card Replaceable Parts List

| REFERENCE DESIGNATION | HP PART NO. | DESCRIPTION | MFR CODE | MFR PART NO. |
|---|---|---|---|---|
| C1,2,3,11,19,20,21 | 0180-0291 | Capacitor, Fxd, Tant, 1.0 uF, 10% | 56289 | 150D105X9035A2 |
| C8 | 0121-0046 | Capacitor, Variable, 9 to 35 pF | 72982 | 538-011-E2PO-94R |
| C9* | 0160-2101 | Capacitor, Fxd, Mica, 27 pF, 5% | 72136 | RDM15E270G3C |
| C9* | 0160-0356 | Capacitor, Fxd, Mica, 18 pF, 5% | 28480 | 0160-0356 |
| C9* | 0160-2197 | Capacitor, Fxd, Mica, 10 pF, 5% | 72136 | RDM15C100J3C |
| C10 | 0140-0149 | Capacitor, Fxd, Mica, 470 pF, 5% | 72136 | DM15F471J |
| C12 | 0160-0153 | Capacitor, Fxd, Mylar, 0.001 uF, 10% | 56289 | 192P10292-PTS |
| C13 | 0160-0134 | Capacitor, Fxd, Mica, 220 pF, 5% | 72136 | DM15F221J (300V) |
| CR1* | 1901-0040 | Diode, Silicon, 30 mA, 30V | 07263 | FDG1088 |
| MC15,25,35,45,97 | 1820-0954 | Integrated Circuit, CTL | 07263 | SL3457 |
| MC17,107 | 1820-0956 | Integrated Circuit, CTL | 07263 | SL3459 |
| MC23,33,43,53,63,73,83,93 | 1820-0055 | Integrated Circuit, TTL | 01295 | SN4356 |
| MC27,57,65,75,85,95,115,127 | 1820-0952 | Integrated Circuit, CTL | 07263 | SL3455 |
| MC37,47,55,77,87,105,117, 123,125 | 1820-0953 | Integrated Circuit, CTL | 07263 | SL3456 |
| MC67 | 1820-0967 | Integrated Circuit | 28480 | 1820-0967 |
| MC113 | 1820-0205 | Integrated Circuit | 28480 | 1820-0205 |
| Q1 | 1854-0019 | Transistor, Silicon, NPN (S6515) | 28480 | 1854-0019 |
| Q2 thru Q5 | 1854-0094 | Transistor, Silicon, NPN (2N3646) | 07263 | 2N3646 |
| R9 | 0683-6835 | Resistor, Fxd, 68k, 5%, 1/4W | 01121 | CB6835 |
| R10,20 | 0683-1035 | Resistor, Fxd, 10k, 5%, 1/4W | 01121 | CB1035 |
| R11 | 0683-4705 | Resistor, Fxd, 47 ohms, 5%, 1/4W | 01121 | CB4705 |
| R12 | 0683-8225 | Resistor, Fxd, 8.2k, 5%, 1/4W | 01121 | CB8225 |
| R13 | 0683-2225 | Resistor, Fxd, 2.2k, 5%, 1/4W | 01121 | CB2225 |
| R14 | 0683-3335 | Resistor, Fxd, 33k, 5%, 1/4W | 01121 | CB3335 |
| R15 | 0683-3925 | Resistor, Fxd, 3.9k, 5%, 1/4W | 01121 | CB3925 |
| R16 | 0683-2725 | Resistor, Fxd, 2.7k, 5%, 1/4W | 01121 | CB2725 |
| R17 | 0683-1515 | Resistor, Fxd, 150 ohms, 5%, 1/4W | 01121 | CB1515 |
| R18 | 0683-1825 | Resistor, Fxd, 1.8k, 5%, 1/4W | 01121 | CB1825 |
| R19,21 | 0683-6825 | Resistor, Fxd, 6.8k, 5%, 1/4W | 01121 | CB6825 |
| R22 | 0683-4725 | Resistor, Fxd, 4.7k, 5%, 1/4W | 01121 | CB4725 |
| R23,25,26,28 | 0683-4715 | Resistor, Fxd, 470 ohms, 5%, 1/4W | 01121 | CB4715 |
| R24,27,29,30 | 0683-1025 | Resistor, Fxd, 1k, 5%, 1/4W | 01121 | CB1025 |
| T1 | 5212A-9A | Transformer | 28480 | 5212A-9A |
| W1 | 8159-0005 | Jumper Wire | 28480 | 8159-0005 |
| Y1 | 0410-0021 | Crystal, Quartz, 100 kHz | 28480 | 0410-0021 |

*First used on card rev. 1147.




NOTE: CR1 NOT USED ON CARD REV. A1028-22




NOTES:

1. 

INTEGRATED CIRCUIT PACK CONNECTIONS FOR MC57, MC65, MC75, MC85, MC95, MC115, AND MC127.

2. DECADE DIVIDER CONNECTIONS:




3. JUMPER W1 POSITION B, IS USED ONLY DURING TESTING.
4. * C9 FACTORY SELECTED NOMINAL VALUE SHOWN.
5. ALL LOGIC POSITIVE-TRUE.
6. ALL RESISTANCE VALUES ARE EXPRESSED IN OHMS.
7. CR1 FIRST USED ON CARD REV. 1147.

Figure 4-2. Time Base Generator Card Parts Location and Logic Diagram

# SECTION V

# REPLACEABLE PARTS

## 5-1. INTRODUCTION.

5-2. This section provides information for ordering replacement parts for the 12539B Time Base Generator Interface Kit. Table 5-1 is a numerical listing of all replaceable parts in the interface kit.

5-3. A time base generator card replaceable parts list (table 4-1) and a parts location diagram (figure 4-2) are provided in section IV of this manual.

5-4. Tables 4-1 and 5-1 list the following information for each replaceable part:

a. Reference designation of the part (table 4-1 only). (Refer to table 5-3 for an explanation of the abbreviations used in the REFERENCE DESIGNATION column.)

b. Hewlett-Packard part number.

c. Description of the part. (Refer to table 5-3 for an explanation of the abbreviations used in the DESCRIPTION column.)

d. A five digit code that corresponds to the manufacturer of the part. (Refer to table 5-2 for the code list of manufacturers.)

e. Manufacturers part number.

f. Total quantity (TQ) of each part used in the kit or assembly (table 5-1 only).

## 5-5. ORDERING INFORMATION.

5-6. To order replacement parts, address the order or inquiry to the nearest Hewlett-Packard Sales and Service Office. Refer to the list at the back of this manual for addresses. Specify the following information for each part ordered:

a. Identification of the instrument, kit, or assembly containing the part (refer to paragraphs 1-8 through 1-10).

b. Hewlett-Packard part number for each part.

c. Description of each part.

d. Circuit reference designation for each part (if applicable).

Table 5-1. Numerical List of Replaceable Parts

| HP PART NO. | DESCRIPTION | MFR CODE | MFR PART NO. | TQ |
|---|---|---|---|---|
| 0121-0046 | Capacitor, Variable, 9 to 35 pF | 72982 | 538-011-E2PO-94R | 1 |
| 0140-0149 | Capacitor, Fxd, Mica, 470 pF, 5% | 72136 | DM15F471J | 1 |
| 0160-0134 | Capacitor, Fxd, Mica, 220 pF, 5% | 72136 | DM15F221J (300V) | 1 |
| 0160-0153 | Capacitor, Fxd, Mylar, 0.001 uF, 10% | 56289 | 192P10292-PTS | 1 |
| 0160-0356 | Capacitor, Fxd, Mica, 18 pF, 5% | 28480 | 0160-0356 | * |
| 0160-2101 | Capacitor, Fxd, Mica, 27 pF, 5% | 72136 | RDM15E270G3C | * |
| 0160-2197 | Capacitor, Fxd, Mica, 10 pF, 5% | 72136 | RDM15C100J3C | * |
| 0180-0291 | Capacitor, Fxd, Tant, 1.0 uF, 10% | 56289 | 150D105X9035A2 | 7 |
| 0410-0021 | Crystal, Quartz, 100 kHz | 28480 | 0410-0021 | 1 |
| 0683-1025 | Resistor, Fxd, 1k, 5%, 1/4W | 01121 | CB1025 | 4 |
| 0683-1035 | Resistor, Fxd, 10k, 5%, 1/4W | 01121 | CB1035 | 2 |
| 0683-1515 | Resistor, Fxd, 150 ohms, 5%, 1/4W | 01121 | CB1515 | 1 |
| 0683-1825 | Resistor, Fxd, 1.8k, 5%, 1/4W | 01121 | CB1825 | 1 |
| 0683-2225 | Resistor, Fxd, 2.2k, 5%, 1/4W | 01121 | CB2225 | 1 |
| 0683-2725 | Resistor, Fxd, 2.7k, 5%, 1/4W | 01121 | CB2725 | 1 |
| 0683-3335 | Resistor, Fxd, 33k, 5%, 1/4W | 01121 | CB3335 | 1 |
| 0683-3925 | Resistor, Fxd, 3.9k, 5%, 1/4W | 01121 | CB3925 | 1 |
| 0683-4705 | Resistor, Fxd, 47 ohms, 5%, 1/4W | 01121 | CB4705 | 1 |
| 0683-4715 | Resistor, Fxd, 470 ohms, 5%, 1/4W | 01121 | CB4715 | 4 |
| 0683-4725 | Resistor, Fxd, 4.7k, 5%, 1/4W | 01121 | CB4725 | 1 |
| 0683-6825 | Resistor, Fxd, 6.8k, 5%, 1/4W | 01121 | CB6825 | 2 |
| 0683-6835 | Resistor, Fxd, 68k, 5%, 1/4W | 01121 | CB6835 | 1 |
| 0683-8225 | Resistor, Fxd, 8.2k, 5%, 1/4W | 01121 | CB8225 | 1 |
| 1200-0199 | Socket, Crystal | 91506 | 8000-AG8 | |
| 1820-0055 | Integrated Circuit, TTL | 01295 | SN4356 | 8 |
| 1820-0205 | Integrated Circuit, TTL | 28480 | 1820-0205 | 1 |
| 1820-0952 | Integrated Circuit, CTL | 07263 | SL3455 | 8 |
| 1820-0953 | Integrated Circuit, CTL | 07263 | SL3456 | 9 |
| 1820-0954 | Integrated Circuit, CTL | 07263 | SL3457 | 5 |
| 1820-0956 | Integrated Circuit, CTL | 07263 | SL3459 | 2 |
| 1820-0967 | Integrated Circuit, CTL | 28480 | 1820-0967 | 1 |
| 1854-0019 | Transistor, Silicon, NPN (S6515) | 28480 | 1854-0019 | 1 |
| 1854-0094 | Transistor, Silicon, NPN (2N3646) | 07263 | 2N3646 | 4 |
| 1901-0040 | Diode, Silicon, 30 mA, 30V (Note 2) | 07263 | FDG1088 | 1 |
| 8159-0005 | Jumper Wire | 28480 | 8159-0005 | 1 |
| 5212-9A | Transformer | 28480 | 5212-9A | 1 |
| 12539-60001 | Time Base Generator Interface Card | 28480 | 12539-60001 | 1 |
| 12539-90002 | Operating and Service Manual | 28480 | 12539-90002 | 1 |

NOTES: 1. Only one of the items marked with asterisk in TQ column is supplied with kit. Determined during factory testing.
2. First used on card rev. 1147.

Table 5-2. Code List of Manufacturers

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and their latest supplements.

| Code No. | Manufacturer | Address |
|---|---|---|
| 01121 | Allen Bradley, Co. | Milwaukee, Wis. |
| 01295 | Texas Instruments, Inc., Transistor Products Div. | Dallas, Texas |
| 07263 | Fairchild Camera & Inst. Corp., Semiconductor Div. | Mountain View, Cal. |
| 28480 | Hewlett-Packard Co. | Palo Alto, Cal. |
| 56289 | Sprague Electric Co. | North Adams, Mass. |
| 72136 | Electro Motive Mfg. Co., Inc. | Willimantic, Conn. |
| 72982 | Erie Technological Products, Inc. | Erie, Pa. |
| 91506 | Augat, Inc. | Attleboro, Mass. |


MANUAL PART NO. 12539-90002
MICROFICHE PART NO. 12539-90006

PRINTED IN U.S.A.

HEWLETT PACKARD

# OPERATING AND SERVICE MANUAL

# 12539C

## TIME BASE GENERATOR INTERFACE KIT

(FOR THE 2100 SERIES COMPUTERS)

Printed-Circuit Assembly:

12539-60003, Series 1232

12539-90008

HEWLETT-PACKARD COMPANY
11000 WOLFE ROAD, CUPERTINO, CALIFORNIA, U.S.A.

PRINTED: JAN 1973

HEWLETT hp PACKARD

# 12539C
TIME BASE GENERATOR

# UPDATING SUPPLEMENT FOR OPERATING AND SERVICE MANUAL

18 APR 1973

## MANUAL IDENTIFICATION

Manual Serial No. Prefix: NA

Manual Printed: JAN 1973

Manual Part Number: 12539-90008

## SUPPLEMENT DESCRIPTION

The purpose of this supplement is to adapt the manual to instruments containing production improvements made subsequent to the printing of the manual and to correct manual errors. Enter the new information (or the Change Number, if more convenient) into the appropriate places in the manual, identified at left.

### INSTRUMENT CHANGES

| Serial No. Prefix | Change |
|---|---|
| 1232 | 1 thru 4 |
| | |
| | |
| | |
| | |

### ASSEMBLY CHANGES

| Ref Des | Description | HP Part No. | Rev | Changes |
|---|---|---|---|---|
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

Changes 1 through 4 dated 18 April 1973.



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| CHANGE | DESCRIPTION |
|---|---|
| 1 | Title page. Change the printed-circuit assembly series number to "1315". |
| 2 | Page 4-3. Delete the entries for R1 and R4,5. |
| 3 | Page 4-5. Change the parts location diagram as follows:<br>a. Change card rev. to "A-1315-22".<br>b. At upper-center, delete "R1".<br>c. At right center, delete "R4" and "R5". |
| 4 | Page 4-5. Change the logic diagram as follows:<br>a. At upper left, change card rev. to "1315".<br>b. At upper left, change R4 to "R6A". Change the value to "1.5K".<br>c. At left center, change R5 to "R6B". Change the value to "1.5K".<br>d. At right center, delete resistor R1. |

# CONTENTS

# ILLUSTRATIONS



# TABLES

# SECTION I GENERAL INFORMATION

## 1-1. INTRODUCTION.

1-2. This manual provides general information, installation and programming instructions, theory of operation, maintenance instructions, and replaceable parts information for the Hewlett-Packard 12539C Time Base Generator Interface Kit (figure 1-1).

## 1-3. DESCRIPTION.

1-4. The HP 12539C Time Base Generator measures real-time intervals in decade steps from 0.1 millisecond to 1000 seconds (16.67 minutes). A three-bit control word transferred to the time base generator by programmed instruction selects the time interval to be measured. The 1-MHz crystal-controlled oscillator used as the frequency standard for the time base generator allows generation of timing signals accurate to within 2 seconds per 24-hour day.

1-5. KIT CONTENTS.

1-6. The time base generator interface kit consists of a time base generator printed-circuit assembly, part no. 12539-60003, and the operating and service manual, part no. 12539-60008.

1-7. IDENTIFICATION.

1-8. This operating and service manual is identified on the title page by interface kit designation and nomenclature, printed-circuit assembly part number and series code, manual part number, and publication date. Refer to the information presented in the following paragraphs and ensure that this manual applies to the equipment being serviced.

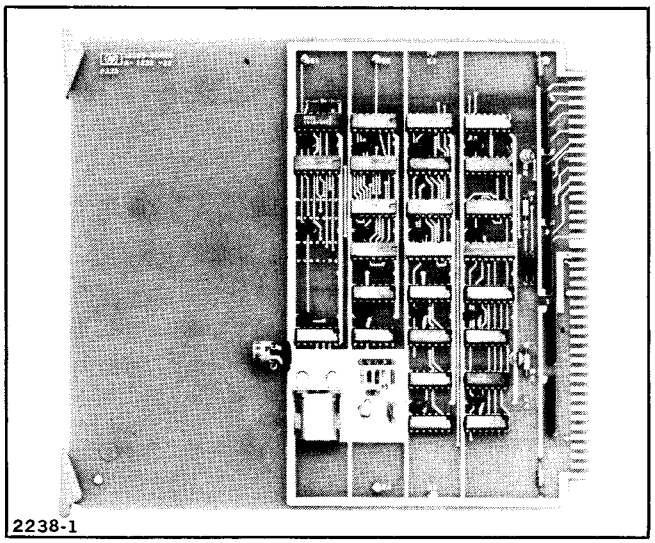



Figure 1-1. HP 12539C Time Base Generator Interface Kit

1-9. Hewlett-Packard uses five digits and a letter (00000A) for standard interface kit designation. If the designation of your kit does not agree with that on the title page of this manual, there are differences between your kit and the kit described in this manual. The appropriate manual or manual supplement is available at the nearest HP Sales and Service Office listed at the back of this manual.

1-10. Printed-circuit assembly (PCA) revisions are identified by a letter, a series code, and a division code stamped on the board (e.g., A-1232-22). The letter code identifies the version of the etched trace pattern on the unloaded board. The series code (four middle digits) refers to the electrical characteristics of the loaded assembly and the positions of the components. The division code (last two digits) identifies the Hewlett-Packard division which manufactured the PCA. If the series code stamped on the PCA does not agree with the series code shown on the title page of this manual, there are differences between your PCA and the PCA described in this manual. These differences are described in change sheets and manual supplements available at the nearest HP Sales and Service Office.

## 1-11. SPECIFICATIONS.

1-12. Table 1-1 lists the specifications for the HP 12539C Time Base Generator Interface PCA.

Table 1-1. Time Base Generator Specifications

| CHARACTERISTICS | SPECIFICATIONS |
|---|---|
| Time Base Intervals: | 0.1 millisecond<br>1 millisecond<br>10 milliseconds<br>100 milliseconds<br>1 second<br>10 seconds<br>100 seconds<br>1000 seconds |
| Time Base Accuracy: | 2 seconds per 24-hour day |
| Current Requirements from Computer Power Supply: | |
| −2V | 0.016A |
| +4.85V | 0.75A |
| Logic Levels | |
| Logic 1 (high): | +2.4 or greater |
| Logic 0 (low): | +0.4V or less |

# SECTION II INSTALLATION AND PROGRAMMING

## 2-1. INTRODUCTION.

2-2. This section provides information for unpacking and inspection, reshipment, installation, and programming the HP 12539C Time Base Generator Interface Kit.

## 2-3. UNPACKING AND INSPECTION.

2-4. If the shipping carton is damaged upon receipt, request that the carrier's agent be present when the card is unpacked. Inspect the PCA for damage (cracks, broken components, etc.). If the PCA is damaged and fails to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing material for the carrier's inspection. The HP Sales and Service Office will arrange for repair or replacement of the damaged PCA without waiting for claims against the carrier to be settled.

## 2-5. RESHIPMENT.

2-6. If an item of the kit is to be shipped to Hewlett-Packard for service or repair, attach a tag to the item identifying the owner and indicating the service or repair to be accomplished. Include the model number of the kit.

2-7. Pack the item in the original factory packing material if available. If the original material is not available, standard factory packing material can be obtained from the nearest Hewlett-Packard Sales and Service Office.

2-8. If standard packing material is not used, wrap the item in Air Cap TH-240 cushioning (manufactured by Sealed Air Corporation, Hawthorn, N.J.) or equivalent and place in a corrugated carton (200 pound test material). Seal the shipping carton securely and mark it "FRAGILE" to ensure careful handling.

Note: In any correspondence, identify the kit by number. Refer any questions to the nearest Hewlett-Packard Sales and Service Office.

## 2-9. INSTALLATION.

2-10. The time base generator PCA obtains its operating currents from the computer power supply. Before installing the PCA, determine the current requirements of this PCA in combination with all other interface or accessory kits already installed in the computer. The computer system documentation defines the currents available from the computer and describes the procedures for calculating the total power supply current requirements. If the total current requirements exceed the limitations of the computer power supply, a Hewlett-Packard power supply extender unit or input/output extender unit must be used. See table 1-1 for the current requirements of the time base generator PCA.

2-11. After ensuring sufficient power, install the time base generator PCA as follows:

a. Turn power off at the computer.

b. Insert the time base generator PCA in the computer I/O slot corresponding to the desired select code.

c. Turn on power and perform the diagnostic program procedure (part no. 12539-90005 for 2100A Computers or part no. 12539-90003 for 2114, 2115, and 2116 Computers) contained in the Manual of Diagnostics to verify proper operation of the time base generator PCA.

d. Check the oscillator output frequency at test point E4 using a Hewlett-Packard 5244L Electronic Counter or equivalent. The frequency should be 1-MHz ± 0.5 Hz. If the frequency is not within tolerance, adjust the frequency according to the oscillator adjustment procedures given in paragraph 4-10.

## 2-12. PROGRAMMING.

2-13. CONTROL WORD.

2-14. The desired time interval to be measured by the time base generator is selected by transferring a three-bit control word from the computer A- or B-register to the time base generator. Table 2-1 lists the possible control word bit combinations and the time interval selected by each. Note that the time intervals are selected in increments equal to $10^{n-1}$ milliseconds where n is the decimal equivalent of the three-bit control word. For non-decade time intervals a decade interval must be counted by software to form the desired interval. For example, if a time interval of three milliseconds is desired, a one millisecond interval must be counted by software three times, to obtain the desired interval.

2-15. ERROR CHECK.

2-16. When more than one decade time interval is required for any given timing operation, the time base generator provides a means of ensuring that all selected intervals have been acknowledged by the computer. A status word, transferred from the time base generator to the computer A- or B-register by an LIA or LIB instruction, contains a single significant bit (bit 4). If this bit is a logic 1, at least

one time interval has been lost. This status word should be checked by software after each decade time interval.

2-17. Jumper W1 on the PCA can be placed in position B to make bit 5 significant also. In this way, bit 5 can be checked by software to determine if a time interval has been lost.

2-18. SAMPLE PROGRAM.

2-19. Table 2-2 is a sample program demonstrating the operation of the time base generator. Under control of this program, the time base generator will provide a measured time interval of 5 seconds. This is done by counting five 1-second intervals with a software counter. After each 1-second interval, the error status bit is checked to ensure that all of the 1-second intervals are acknowledged by the computer.

Table 2-1. Control Word Combinations and Time Intervals

| CONTROL WORD | | | SELECTED TIME INTERVAL |
|---|---|---|---|
| BIT 2 | BIT 1 | BIT 0 | |
| 0 | 0 | 0 | 0.1 millisecond |
| 0 | 0 | 1 | 1 millisecond |
| 0 | 1 | 0 | 10 milliseconds |
| 0 | 1 | 1 | 100 milliseconds |
| 1 | 0 | 0 | 1 second |
| 1 | 0 | 1 | 10 seconds |
| 1 | 1 | 0 | 100 seconds |
| 1 | 1 | 1 | 1000 seconds |

NOTE: Bits 3 through 15 not used.

Table 2-2. Sample Program

```
0001                        ASMB,A,B,L,T
0002*
0003*   THIS IS A SAMPLE PROGRAM TO DEMONSTRATE THE OPERATION OF THE
0004*   TIME BASE GENERATOR. UNDER CONTROL OF THIS PROGRAM, THE TIME
0005*   BASE GENERATOR WILL PROVIDE A MEASURED INTERVAL OF FIVE SECONDS.
0006*   THIS REQUIRES THAT FIVE DECADE INTERVALS OF ONE SECOND EACH
0007*   BE MEASURED AND COUNTED BY SOFTWARE. AFTER EACH DECADE INTERVAL
0008*   IS MEASURED, THE ERROR STATUS IS CHECKED AND IF AN ERROR IS
0009*   DETECTED, THE COMPUTER HALTS WITH A T-REGISTER DISPLAY OF
0010*   102066 OCTAL.
0011*
0012    00100                       ORG     100B
0013*
0014    00100   000000    START     NOP
0015    00101   060121              LDA     .5          INITIALIZE COUNTER TO COUNT
0016    00102   070122              STA     COUNT       FIVE DECADE INTERVALS.
0017*
0018*   THIS PART OF THE PROGRAM OPERATES THE TIME BASE GENERATOR.
0019*
0020    00103   060123              LDA     CW          GET CONTROL WORD AND TRANSFER
0021    00104   102615              OTA     TBG         TO TIME BASE GENERATOR.
0022    00105   102715              STC     TBG         START TIME BASE GENERATOR
0023    00106   103115    GO        CLF     TBG         ENABLE FLAG LOGIC.
0024    00107   102315              SFS     TBG         HAS DECADE INTERVAL ELAPSED?
0025    00110   024107              JMP     *-1         NO. WAIT.
0026    00111   024112              JMP     STAT        YES. CHECK ERROR STATUS.
0027*
0028*   THIS PART OF THE PROGRAM CHECKS ERROR STATUS AND INCREMENTS
0029*   THE DECADE INTERVAL COUNTER.
0030*
0031    00112   102515    STAT      LIA     TBG         GET STATUS WORD FROM TIME BASE
0032*                                                       GENERATOR
0033    00113   050124              CPA     ERR         DOES STATUS WORD INDICATE AN ERROR?
0034    00114   102066              HLT     66B         YES. HALT COMPUTER.
0035    00115   034122              ISZ     COUNT       NO. INCREMENT COUNTER. IS TIME
0036*                                                       INTERVAL COMPLETE?
0037    00116   024106              JMP     GO          NO. START ANOTHER DECADE INTERVAL.
0038    00117   106715              CLC     TBG         YES. STOP DECADE COUNTERS.
0039    00120   102077              HLT     77B         HALT COMPUTER.
0040*
0041*   CONSTANT AND STORAGE INFORMATION.
0042*
0043    00121   177773    .5        DEC     -5
0044    00122   000000    COUNT     BSS     1
0045    00123   000004    CW        OCT     4
0046    00124   000020    ERR       OCT     20
0047    00015             TBG       EQU     158
0048*
0049                                END     START
**      NO ERRORS*
```

# SECTION III THEORY OF OPERATION

## 3-1. INTRODUCTION.

3-2. This section provides functional and detailed theory of operation for the HP 12539C Time Base Generator Interface Kit.

## 3-3. FUNCTIONAL THEORY OF OPERATION.

3-4. Figure 3-1 is a block diagram of the time base generator PCA and a flowchart showing the functional operation of the time base generator PCA. The program instructions shown in the flowchart are the same as those used in the sample program in table 2-2 in section II of this manual.

3-5. Operation of the time base generator begins with the transfer of a three-bit control word from the computer A- or B-register to the time base selection register with an OTA or OTB instruction. The next instruction (STC,C) causes a shaped 100-kHz signal to be gated to the decade divider circuits. This marks the beginning of the time interval.

3-6. An SFS instruction is used to determine if the selected time interval has elapsed. Before the time interval has elapsed, a JMP *-1 instruction is executed followed by the SFS instruction again. This wait loop continues until the selected time interval has elapsed.

3-7. At the end of the selected time interval, the time base generator supplies an SKF signal. The SKF signal causes the computer to skip the JMP *-1 instruction and proceed with the program. The time spent in the wait loop is the time selected by the control word that was initially transferred to the time base generator.

## 3-8. DETAILED THEORY OF OPERATION.

3-9. Refer to the time base generator logic diagram, figure 4-2, in section IV of this manual while reading the detailed theory of operation discussion.

3-10. For an index of signals on the 86-pin edge of the time base generator PCA, refer to the computer system documentation.

3-11. All logic levels on the time base generator PCA are positive-true. The term "high" refers to a level of approximately +2.4V and "low" refers to approximately +0.4V. These signal levels vary somewhat depending on the integrated circuit package involved.

3-12. POWER-ON LOGIC.

3-13. When power is initially applied to the computer or the computer PRESET switch is pressed, the computer supplies a POPIO and a CRS signal to the time base generator PCA. The POPIO signal sets the Flag Buffer FF and the CRS signal clears the Control FF. An ENF signal at the next computer time T2 is gated with the set-side output of the Flag Buffer FF to set the Flag FF. The low set-side output of the Control FF is applied through U34D to the clear inputs of the decade dividers ensuring that they are initially in the clear state. The low set-side output of the Control FF also inhibits "and" gate U24D to prevent the 100-kHz signal from clocking the decade dividers. Also, the first ENF signal clears the IRQ FF. Because the output of the eight-to-one multiplexer circuit is low, the Time Flag FF clears when the first SIR signal is received at computer time T5.

3-14. TIME STANDARD LOGIC.

3-15. The basic component of the time standard logic is a 1-MHz crystal oscillator accurate to 20 ppm (parts per million). The 1-MHz signal is applied to decade divider U75 to obtain a 100-kHz signal. "And" gate U24D allows the control logic to control the application of this 100-kHz signal to the decade dividers as described in paragraph 3-24.

3-16. The gated 100-kHz signal is applied to the first of the eight decade dividers. The decade dividers are wired externally to operate as binary coded decimal counters with a count added each time the input signal (pin 14) swings low. The output signal (pin 11) swings high on the eighth count then low on the tenth count. The low swing adds one count to the next divider stage. The output signals from each of the decade dividers are applied to the time base selection logic.

3-17. TIME BASE SELECTION LOGIC.

3-18. The time base selection logic consists of three Time Base Selection FF's (BIT 0-3 FF's) and an eight-to-one multiplexer circuit.

3-19. The desired time interval to be measured by the time base generator PCA is encoded into a three-bit control word. This control word is transferred from the computer A- or B-register to the Time Base Selection FF's by an OTA or OTB instruction with the select code of the time base generator. Either of these instructions supply high SCM, SCL, IOG, and IOO signals and the three-bit control word (IOBO 0, IOBO 1, and IOBO 2) to the time base generator.

3-20. When the IOO signal goes high at computer time T3, the three-bit control word is stored in the Time Base Selection FF's. The IOO signal also clears all nine decade dividers and the Control FF at this time.

3-21. The outputs of the Time Base Selection FF's control the eight-to-one multiplexer circuit. This circuit decodes the control word so that one of the eight decade dividers is selected as the time base (for time interval).

3-22. CONTROL LOGIC.

3-23. After the control word has been loaded into the Time Base Selection FF's, the time base generator is ready to begin measuring the time period. An STC,C instruction with the select code of the time base generator marks the beginning of the time period. As a result of this instruction, the time base generator PCA receives high IOG, SCM, SCL, STC, and CLF signals from the computer.

3-24. The STC signal sets the Control FF. The high set-side output of the Control FF gates the 100-kHz signal to the decade dividers and provides one of the enabling signals to the time flag gate (U36C).

3-25. The CLF signal clears the Flag Buffer and Flag FF's. The high clear-side output of the Flag FF provides another enabling signal to the time flag gate. (Because the clear-side output of the Time Flag FF is also high, the output of the time flag gate goes high at this time. However, this has no effect since the CLF signal provides an overriding clear signal to the Flag Buffer FF.) The decade dividers are now counting the 100-kHz signal and continue to count until the selected time interval has elapsed.

3-26. FLAG LOGIC.

3-27. The flag logic monitors the output of the eight-to-one multiplexer circuit for a signal indicating the end of the desired time interval.

3-28. For discussion purposes, assume that the control word specifies a time interval of one second. In this instance, the eight-to-one multiplexer selects the U86 decade divider as the time base. When the decade dividers have counted 0.8 second, the output of divider U86 goes high (paragraph 3-16). This signal is gated through the eight-to-one multiplexer circuit to the set input of the Time Flag FF. At the next computer time T5 (SIR), the Time Flag FF sets causing the output of the time flag gate to go low. At the count of one second, the output of divider U86 goes low. The Time Flag FF clears at the next SIR signal causing the output of the time flag gate to go high, setting the Flag Buffer FF. At the next computer time T2 (ENF), the Flag FF sets.

3-29. When the Flag FF is in the set state, the time base generator PCA generates an SRQ signal and, if programmed to do so, generates FLG and IRQ signals or an SKF signal. These signals indicate to the computer that the requested time interval has ended. The following paragraphs describe how these signals are generated and how they are used by the computer.

3-30. SKIP-ON-FLAG SIGNAL. If the computer is programmed to wait for the Flag FF to be set (SFS instruction followed by a JMP *-1 instruction for example), the resulting SFS signal gated with the set side of the Flag FF generates an SKF signal. This causes the computer to skip the next programmed instruction (JMP *-1) and proceed with the program. Figure 3-2 illustrates the generation of an SKF signal by the time base generator PCA. Notice that SKF signal can also be generated when the Flag FF is in the clear state by programming a SFC instruction. Either way, the state of the Flag FF is being tested and the computer must be programmed to respond accordingly.

3-31. INTERRUPT SIGNALS. If the computer interrupt system has been enabled by an STF 00 instruction, the time base generator can be used to generate timed interrupts. Figure 3-3 illustrates the functions involved in an interrupt operation. To interrupt the main program at the end of a measured time interval, the following conditions must be met at the time base generator PCA:

a. Control FF set (paragraph 3-24).

b. Flag Buffer FF set (paragraph 3-28).

c. Flag FF set (paragraph 3-28).

d. IEN signal high (interrupt system enabled).

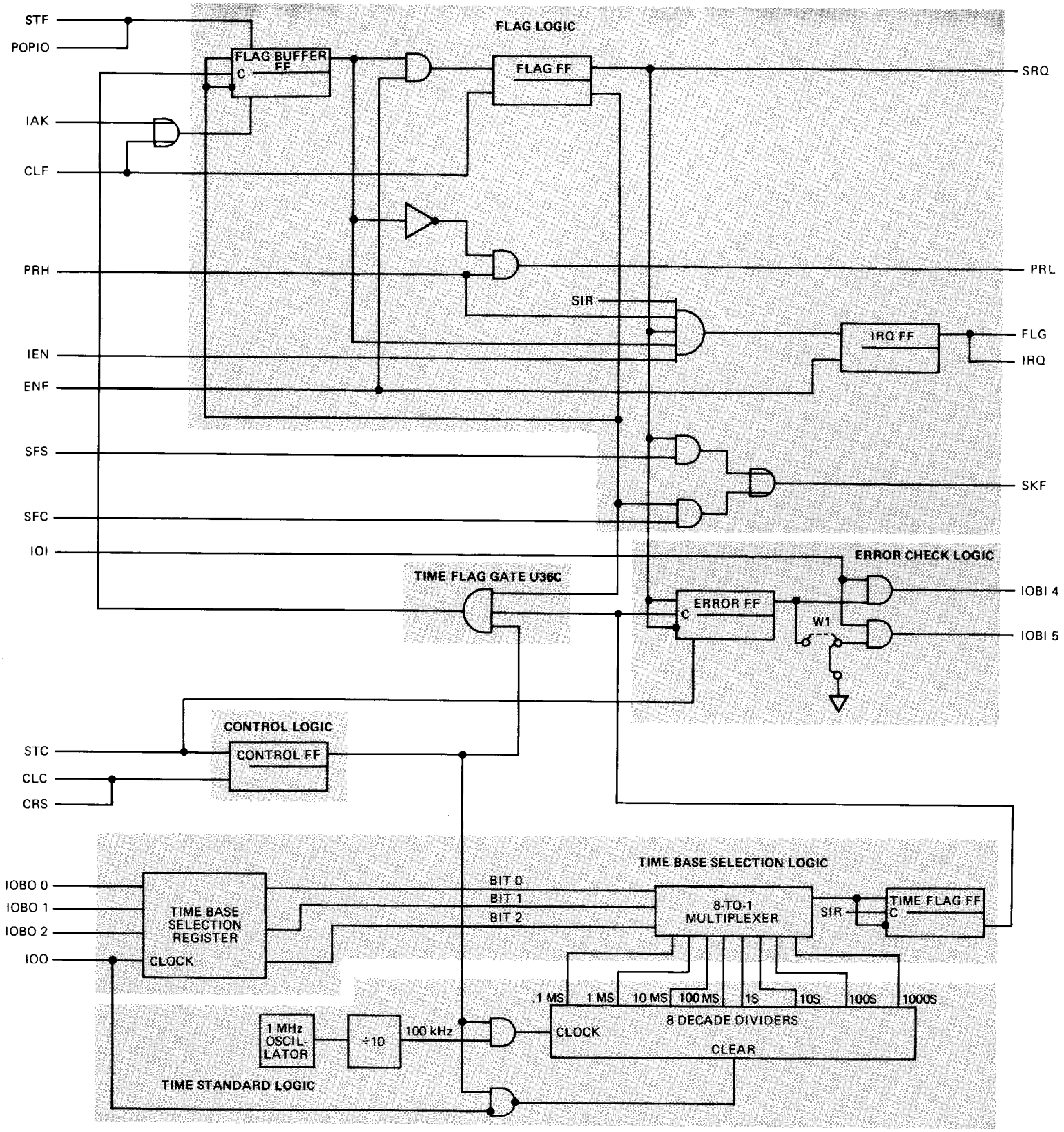
e. PRH signal high (no higher priority interrupts).

3-32. When all of these conditions are established, an SIR signal at time T5 sets the IRQ FF which generates true FLG and IRQ signals. These signals are used by the computer I/O control and addressing circuits to generate an interrupt signal.

3-33. At time T2 following the interrupt, an ENF signal clears the IRQ FF. An SIR signal again sets the IRQ FF if the PRH signal is still high at time T5. The FLG and IRQ signals this time are used by the computer I/O control and addressing circuits to encode the interrupt address.

3-34. The next machine cycle will be under control of the instruction located at the interrupt address in memory. During this machine cycle, an IAK signal at time T6 clears the Flag Buffer FF and an ENF signal at time T2 clears the IRQ FF. The Flag FF remains set to inhibit lower priority interrupts by providing a low PRL signal.

3-35. At this point, the computer normally enters an interrupt subroutine. A CLC instruction is required at the beginning of the subroutine to disable the decade dividers and prevent the Error FF (paragraph 3-37) from being set. Also, just before leaving the subroutine, a CLF instruction is required to enable lower priority interrupts.


STF
POPIO
FLAG LOGIC
FLAG BUFFER FF
C
FLAG FF
SRQ
IAK
CLF
PRH
PRL
SIR
IRQ FF
FLG
IRQ
IEN
ENF
SFS
SKF
SFC
IOI
ERROR CHECK LOGIC
TIME FLAG GATE U36C
ERROR FF
C
W1
IOBI 4
IOBI 5
CONTROL LOGIC
CONTROL FF
STC
CLC
CRS
TIME BASE SELECTION LOGIC
IOBO 0
IOBO 1
IOBO 2
IOO
TIME BASE SELECTION REGISTER
CLOCK
BIT 0
BIT 1
BIT 2
8-TO-1 MULTIPLEXER
SIR
TIME FLAG FF
C
.1 MS
1 MS
10 MS
100 MS
1S
10S
100S
1000S
8 DECADE DIVIDERS
CLOCK
CLEAR
1 MHz OSCIL-LATOR
÷10
100 kHz
TIME STANDARD LOGIC

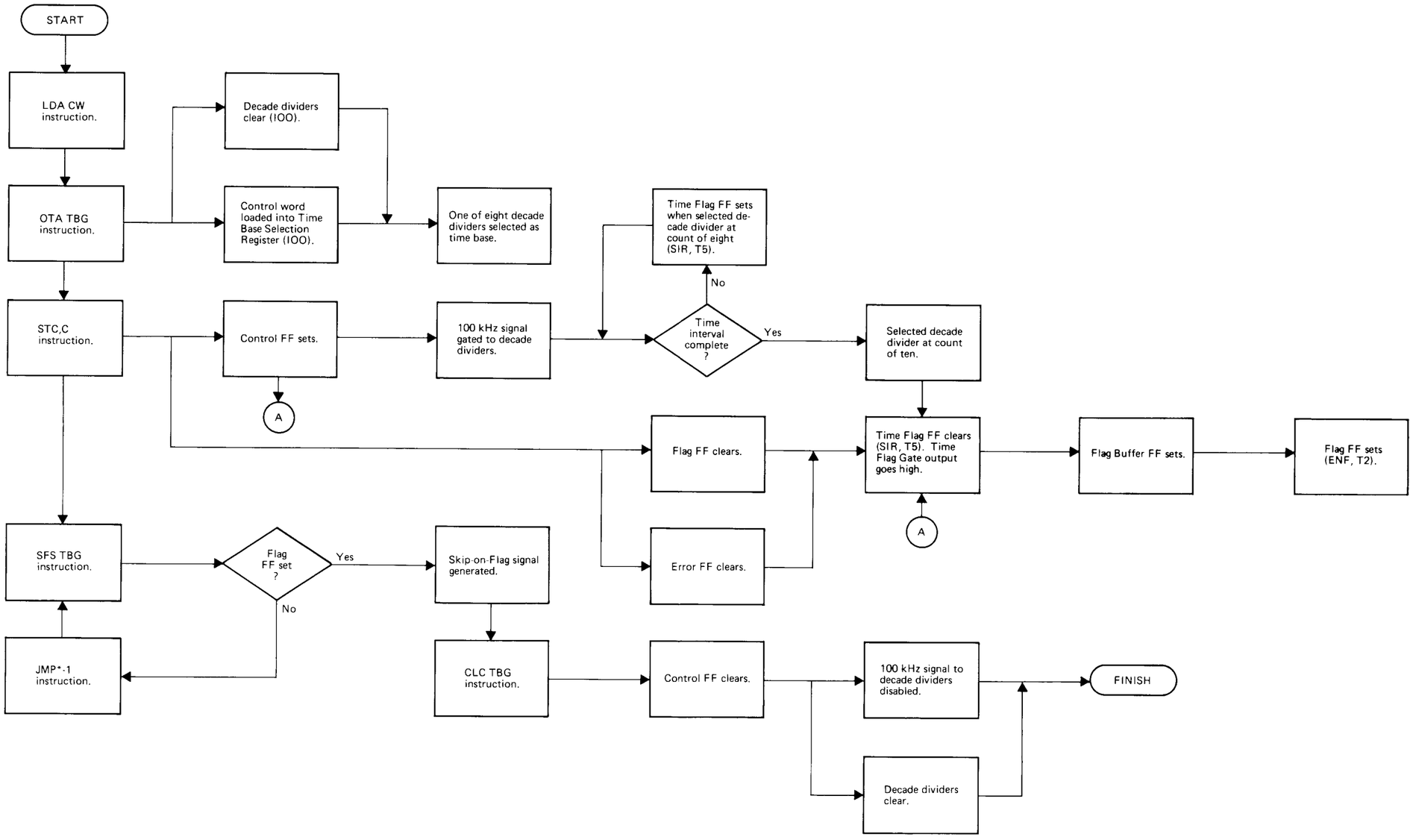



Figure 3-1. Time Base Generator Simplified Logic Diagram and Functional Operation Flowchart

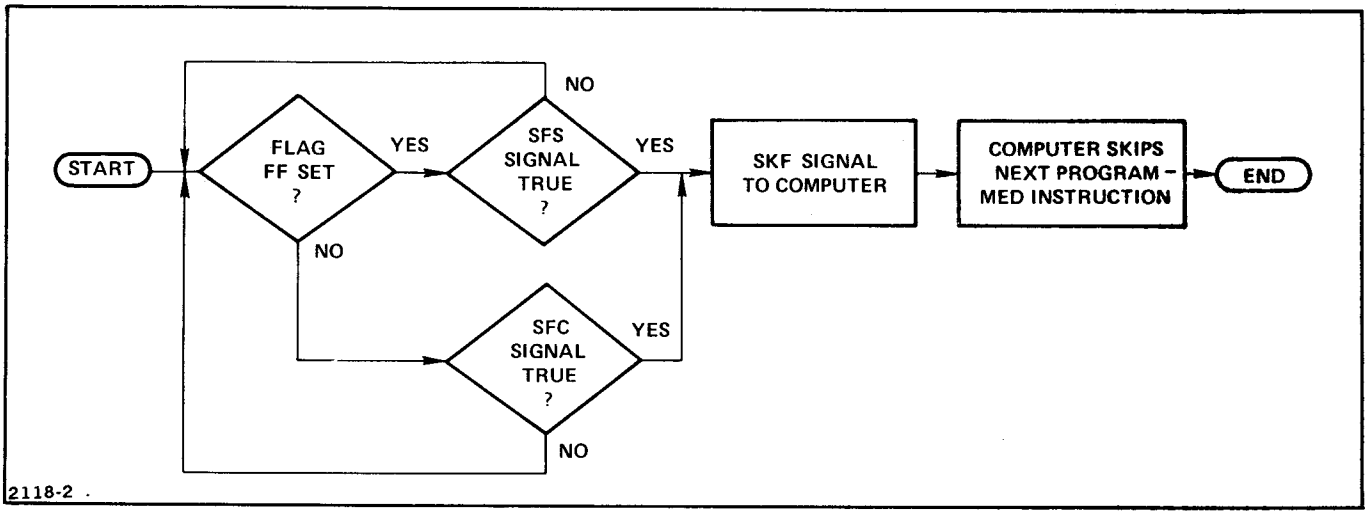



Figure 3-2. Skip-On-Flag Signal Generation Flowchart

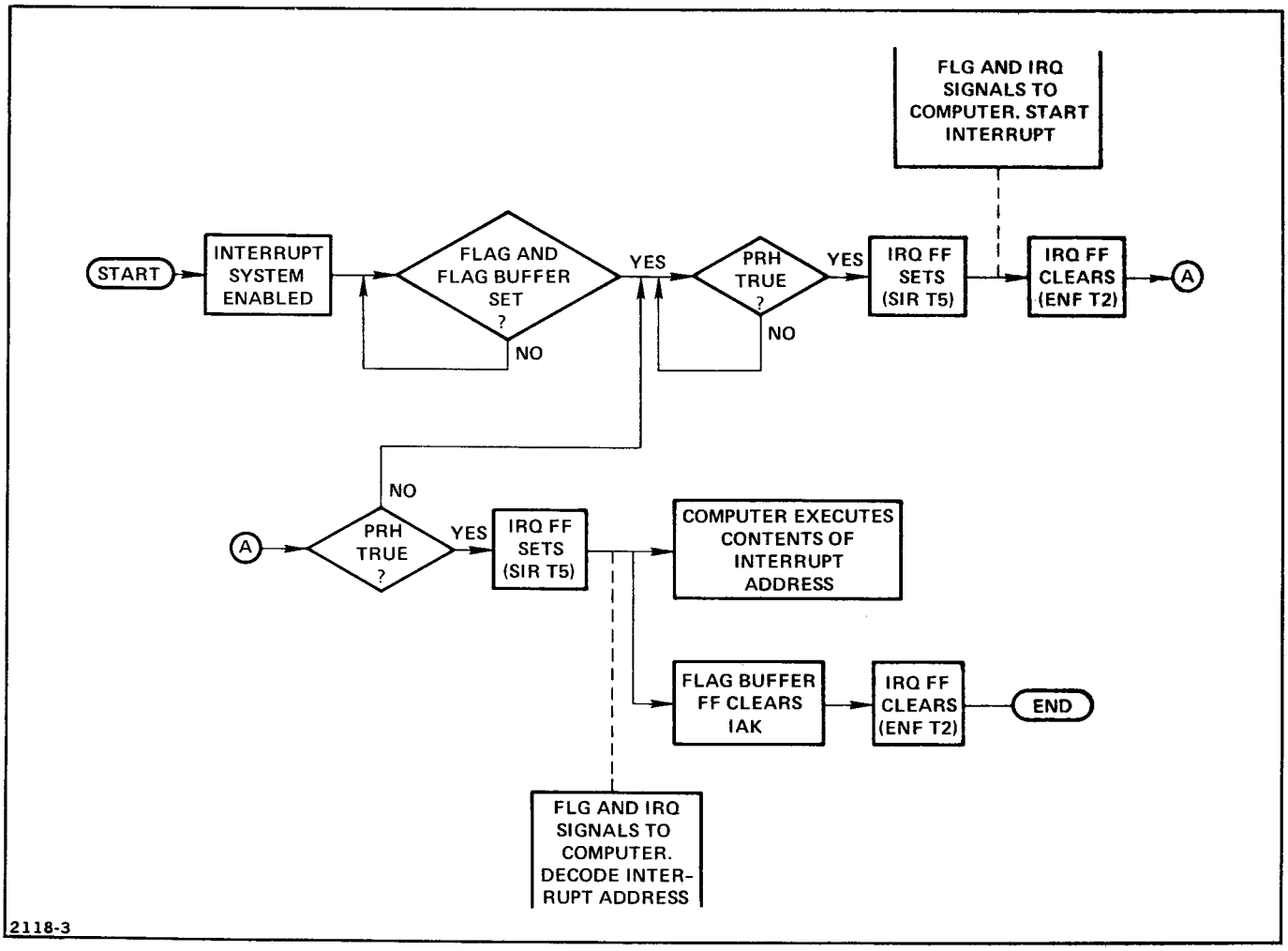



Figure 3-3. Interrupt Operation Flowchart

## 3-36. ERROR CHECK LOGIC.

3-37. The Error FF monitors the set-side output of the Flag FF and is clocked by the clear-side output of the Time Base FF. If the Flag FF is set (indicating that the desired time interval has elapsed) and the selected divider output goes low a second time (causing the Time Flag FF to clear), the Error FF sets.

3-38. The state (set or cleared) of the Error FF is read onto the IOBI 4 line (and the IOBI 5 line if selected by jumper W1) and loaded into the computer A- or B-register by an LIA or LIB instruction addressed to the time base generator. Bit 4 (or 5) of the A- or B-register can then be checked by software for a possible error condition.

# SECTION IV MAINTENANCE

## 4-1. INTRODUCTION.

4-2. This section provides maintenance information for the HP 12539C Time Base Generator Interface Kit. Included are preventive maintenance instructions, troubleshooting instructions, and maintenance data consisting of integrated circuit pin connections (figure 4-1), a time base generator PCA replaceable parts list (table 4-1), and a time base generator PCA parts location and logic diagram (figure 4-2).

## 4-3. PREVENTIVE MAINTENANCE.

4-4. Incorporate preventive maintenance for the time base generator with the preventive maintenance routines for the computer system. Inspect the time base generator PCA for cracked, broken, or burned components, insulation, and connections.

## 4-5. TROUBLESHOOTING.

4-6. Most malfunctions on the time base generator PCA can be traced by performing the diagnostic program procedures (part no. 12539-90005 for 2100A Computers or part no. 12539-90003 for 2114, 2115, and 2116 Computers) contained in the *Manual of Diagnostics* and analyzing error halts as they occur. Use the maintenance data contained in this section to isolate malfunctions to the component level.

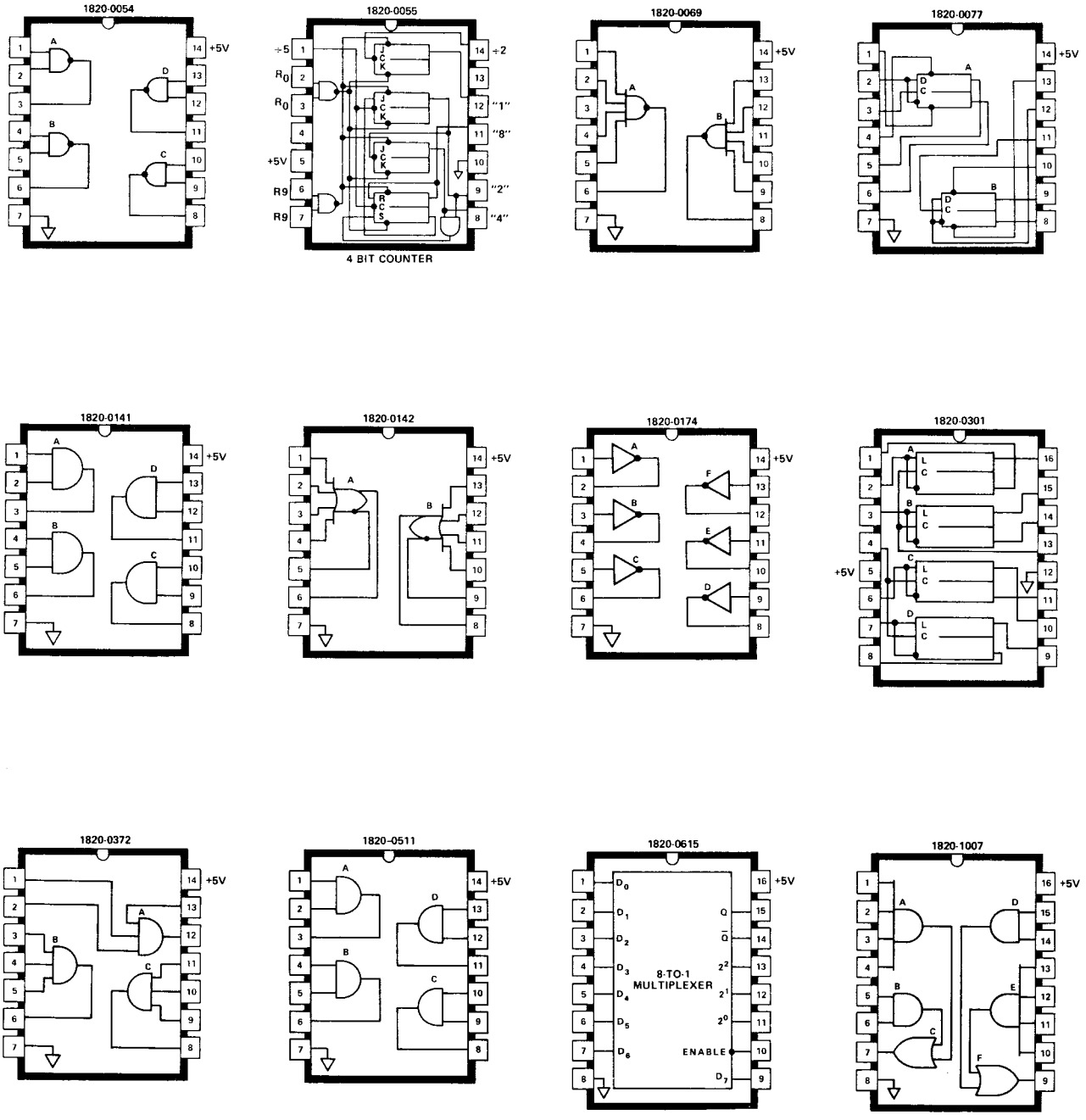
4-7. To facilitate testing the decade dividers, jumper W2 can be moved to position B. This reduces the time interval required to operate the last four divider circuits. With jumper W2 in position B, the decade dividers for 0.1 millisecond (U77), 1 millisecond (U87), 10 milliseconds (U97), and 100 milliseconds (U96) operate normally. However, with jumper W2 in position B, the last four decade dividers operate at 1 millisecond (U86), 10 milliseconds (U76), 100 milliseconds (U66), and 1 second (U65).

Note: If jumper W2 is moved to position B, be sure to return jumper W2 to position A when testing is completed.

4-8. If crystal Y1 is replaced, check the oscillator output frequency at test point E4 using a Hewlett-Packard 5244L Electronic Counter or equivalent. The frequency should be 1-MHz ± 0.5 Hz. If the frequency is not within tolerance, adjust the frequency according to the oscillator adjustment procedures given in paragraph 4-10.

## 4-9. OSCILLATOR ADJUSTMENT.

4-10. Using a Hewlett-Packard 5244L Electronic Counter or equivalent frequency measuring device, observe the oscillator output frequency at test point E4. Adjust capacitor C19 to obtain an output frequency of 1-MHz ±0.5 Hz.

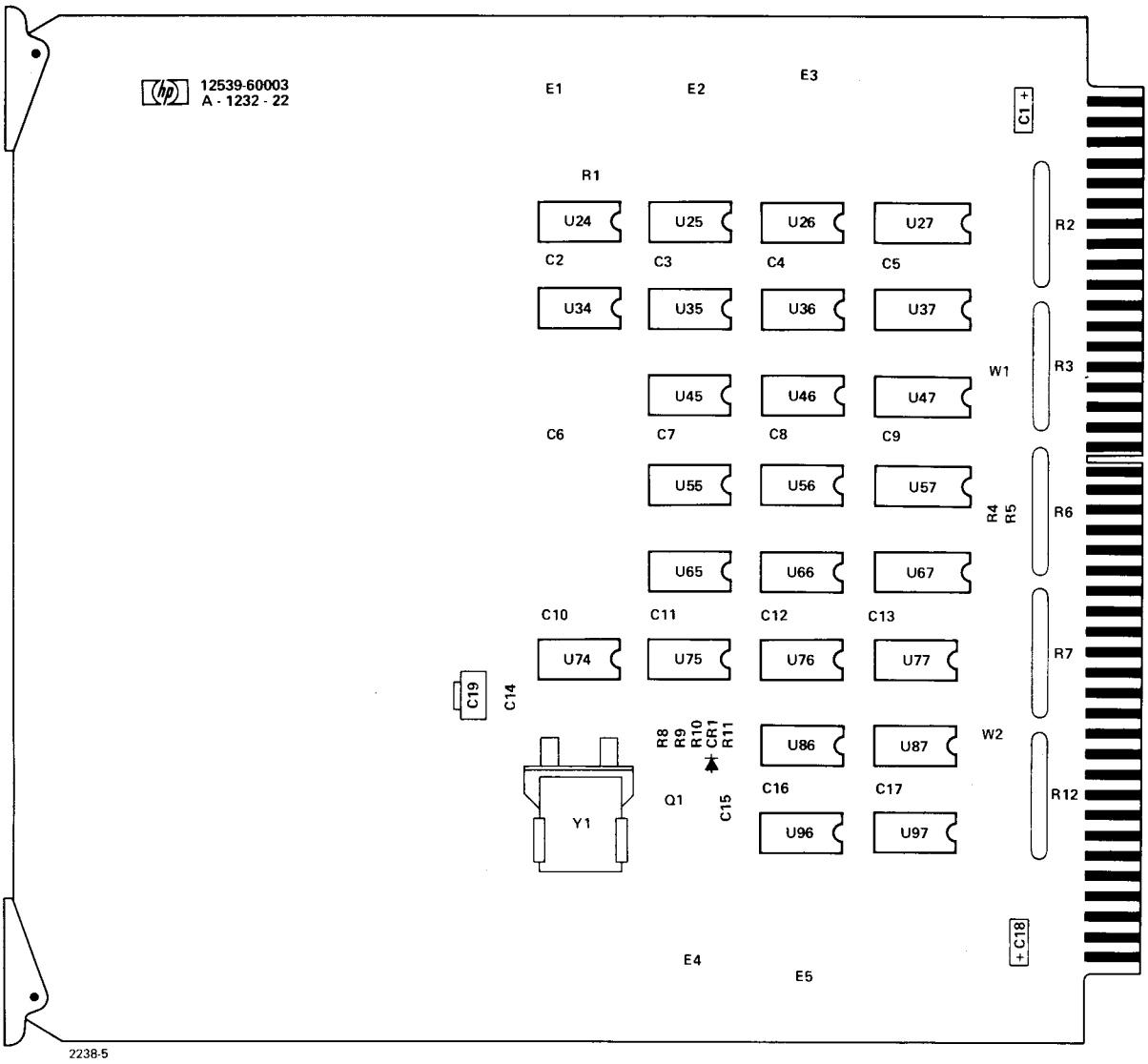



1820-0615: Data on one of the 8 input lines is transferred to the output line when the ENABLE line goes false. The specific input line to be transferred is determined by the three select lines.

Figure 4-1. Integrated Circuit Pin Connections

Table 4-1. Time Base Generator PCA Replaceable Parts

| REFERENCE DESIGNATION | HP PART NO. | DESCRIPTION | MFR CODE | MFR PART NO. |
|---|---|---|---|---|
| | 12539-60003 | TIME BASE GENERATOR PCA | 28480 | 12539-60003 |
| C1, 18 | 0180-0197 | CAPACITOR, fxd, elect, 2.2 μF, 10%, 20 Vdcw | 56289 | 150D225X9020A2-DYS |
| C2 thru C13, C15 thru C17 | 0160-2055 | CAPACITOR, fxd, cer, 0.01 μF, +80 -20%, 100 Vdcw | 56289 | C023F101F103ZS22-CD |
| C14 | 0160-2198 | CAPACITOR, fxd, mica, 20 pF, 5% | 72136 | RDM15C200J3C |
| C19 | 0121-0036 | CAPACITOR, var, cer, 5.5-18 pF | 28480 | 0121-0036 |
| CR1 | 1901-0040 | DIODE, Si, 30 mA, 30WV | 07263 | FDG1088 |
| Q1 | 1850-0158 | TRANSISTOR, Ge, PNP | 80131 | 2N2635 |
| R1 | 0757-0416 | RESISTOR, fxd, flm, 511 ohms, 1%, 1/8W | 28480 | 0757-0416 |
| R2, 3, 6 | 1810-0020 | RESISTOR NETWORK, flm (7 resistor) | 28480 | 1810-0020 |
| R4, 5 | 0757-0420 | RESISTOR, fxd, flm, 750 ohms, 1%, 1/8W | 28480 | 0757-0420 |
| R7, 12 | 1810-0030 | RESISTOR NETWORK, flm (7 resistor 1k, 5%, 0.15W each) | 28480 | 1810-0030 |
| R8 | 0698-3444 | RESISTOR, fxd, flm, 316 ohms, 1%, 1/8W | 28480 | 0698-3444 |
| R9 | 0757-0280 | RESISTOR, fxd, flm, 1k, 1%, 1/8W | 28480 | 0757-0280 |
| R10 | 0698-3440 | RESISTOR, fxd, flm, 196 ohms, 1%, 1/8W | 28480 | 0698-3440 |
| R11 | 0698-3441 | RESISTOR, fxd, flm, 215 ohms, 1%, 1/8W | 28480 | 0698-3441 |
| U24 | 1820-0141 | INTEGRATED CIRCUIT, TTL | 04713 | MC3001P |
| U25, 46 | 1820-0077 | INTEGRATED CIRCUIT, TTL | 01295 | SN7474N |
| U26, 34, 35 | 1820-0054 | INTEGRATED CIRCUIT, TTL | 01295 | SN7400N |
| U27, 37, 47 | 1820-1007 | INTEGRATED CIRCUIT | 28480 | 1820-1007 |
| U36 | 1820-0372 | INTEGRATED CIRCUIT | 28480 | 1820-0372 |
| U45 | 1820-0069 | INTEGRATED CIRCUIT, TTL | 01295 | SN7420N |
| U55 | 1820-0174 | INTEGRATED CIRCUIT, TTL | 01295 | SN7404N |
| U56 | 1820-0511 | INTEGRATED CIRCUIT, TTL | 01295 | SN7408N |
| U57 | 1820-0301 | INTEGRATED CIRCUIT, TTL | 01295 | SN7475N |
| U65, 66, U75 thru U77, 86, 87, 96, 97, | 1820-0055 | INTEGRATED CIRCUIT, TTL | 01295 | SN7490N |
| U67 | 1820-0615 | INTEGRATED CIRCUIT, TTL | 28480 | 1820-0615 |
| U74 | 1820-0142 | INTEGRATED CIRCUIT | 04713 | MC1004P |
| W1, 2 | 8159-0005 | JUMPER, wire | 28480 | 8159-0005 |
| Y1 | 0410-0478 | CRYSTAL, quartz, 1.0 MHz, 32 pF | 28480 | 0410-0478 |


12539-60003
A - 1232 - 22
E1
E2
E3
C1 +
R1
U24
U25
U26
U27
R2
C2
C3
C4
C5
U34
U35
U36
U37
W1
R3
U45
U46
U47
C6
C7
C8
C9
U55
U56
U57
R4
R5
R6
U65
U66
U67
C10
C11
C12
C13
U74
U75
U76
U77
R7
C19
C14
R8
R9
R10
CR1
R11
U86
U87
W2
C16
C17
Q1
C15
Y1
R12
U96
U97
+C18
E4
E5
2238-5

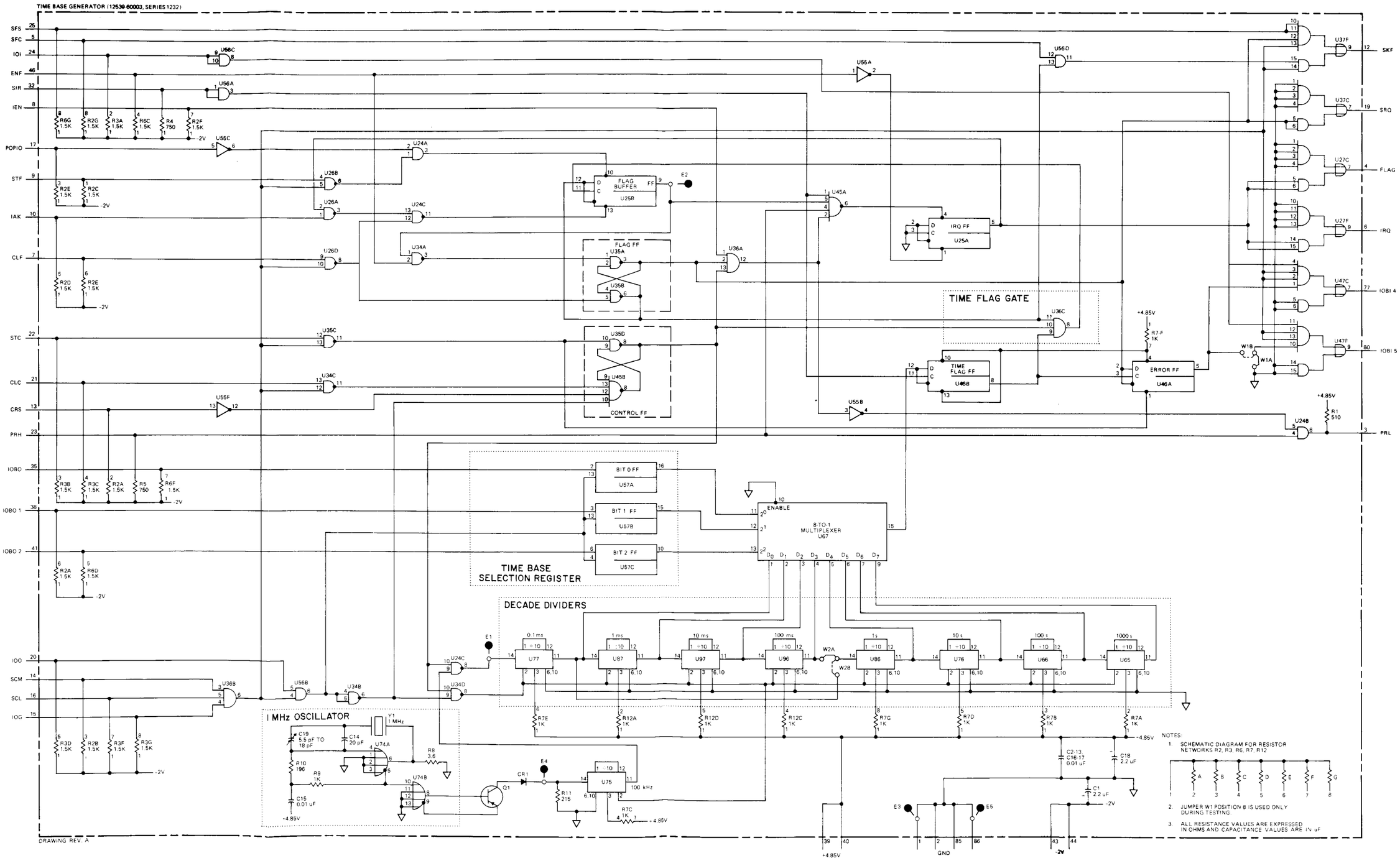



Figure 4-2. Time Base Generator PCA Parts Location and Logic Diagrams

# REPLACEABLE PARTS

SECTION V

## 5-1. INTRODUCTION.

5-2. This section provides information for ordering replacement parts for the HP 12539C Time Base Generator Interface Kit. Table 5-1 is a numerical listing of all replaceable parts in the interface kit.

5-3. A time base generator PCA replaceable parts list (table 4-1) and a parts location diagram (figure 4-2) are provided in section IV of this manual.

5-4. Tables 4-1 and 5-1 list the following information for each replaceable part:

a. Reference designation of the part (table 4-1 only). (Refer to table 5-3 for an explanation of the designations used in the REFERENCE DESIGNATION column.)

b. Hewlett-Packard part number.

c. Description of the part. (Refer to table 5-3 for an explanation of the abbreviations used in the DESCRIPTION column.)

d. A five digit code that corresponds to the manufacturer of the part. (Refer to table 5-2 for the code list of manufacturers.)

e. Manufacturers part number.

f. Total quantity (TQ) of each part used in the kit or assembly (table 5-1 only).

## 5-5. ORDERING INFORMATION.

5-6. To order replacement parts, address the order or inquiry to the nearest Hewlett-Packard Sales and Service Office. Refer to the list at the back of this manual for addresses. Specify the following information for each part ordered:

a. Identification of the kit or assembly containing the part (refer to paragraphs 1-8 through 1-10).

b. Hewlett-Packard part number for each part.

c. Description of each part.

d. Circuit reference designation for each part (if applicable).

Table 5-1. Numerical List of Replaceable Parts

| HP PART NO. | DESCRIPTION | MFR CODE | MFR PART NO. | TQ |
|---|---|---|---|---|
| 0121-0036 | CAPACITOR, var, cer, 5.5-18 pF | 28480 | 0121-0036 | 1 |
| 0160-2055 | CAPACITOR, fxd, cer, 0.01 μF, +80 -20%, 100 Vdcw | 56289 | C023F101F103ZS22-CD | 15 |
| 0160-2198 | CAPACITOR, fxd, mica, 20 pF, 5% | 72136 | RDM15C200J3C | 1 |
| 0180-0197 | CAPACITOR, fxd, elect, 2.2 μF, 10%, 20 Vdcw | 56289 | 150D225X9020A2-DYS | 2 |
| 0410-0478 | CRYSTAL, quartz, 1.0 MHz, 32 pF | 28480 | 0410-0478 | 1 |
| 0698-3440 | RESISTOR, fxd, flm, 196 ohms, 1%, 1/8W | 28480 | 0698-3440 | 1 |
| 0698-3441 | RESISTOR, fxd, flm, 215 ohms, 1%, 1/8W | 28480 | 0698-3441 | 1 |
| 0698-3444 | RESISTOR, fxd, flm, 316 ohms, 1%, 1/8W | 28480 | 0698-3444 | 1 |
| 0757-0280 | RESISTOR, fxd, flm, 1k, 1%, 1/8W | 28480 | 0757-0280 | 1 |
| 0757-0416 | RESISTOR, fxd, flm, 511 ohms, 1%, 1/8W | 28480 | 0757-0416 | 1 |
| 0757-0420 | RESISTOR, fxd, flm, 750 ohms, 1%, 1/8W | 28480 | 0757-0420 | 2 |
| 1810-0020 | RESISTOR NETWORK, flm (7 resistor) | 28480 | 1810-0020 | 3 |
| 1810-0030 | RESISTOR NETWORK, flm (7 resistor 1k, 5%, 0.15W each) | 28480 | 1810-0030 | 2 |
| 1820-0054 | INTEGRATED CIRCUIT, TTL | 01295 | SN7400N | 3 |
| 1820-0055 | INTEGRATED CIRCUIT, TTL | 01295 | SN7490N | 9 |
| 1820-0069 | INTEGRATED CIRCUIT, TTL | 01295 | SN7420N | 1 |
| 1820-0077 | INTEGRATED CIRCUIT, TTL | 01295 | SN7474N | 2 |
| 1820-0141 | INTEGRATED CIRCUIT, TTL | 04713 | MC3001P | 1 |
| 1820-0142 | INTEGRATED CIRCUIT | 04713 | MC1004P | 1 |
| 1820-0174 | INTEGRATED CIRCUIT, TTL | 01295 | SN7404N | 1 |
| 1820-0301 | INTEGRATED CIRCUIT, TTL | 01295 | SN7475N | 1 |
| 1820-0372 | INTEGRATED CIRCUIT, TTL | 28480 | 1820-0372 | 1 |
| 1820-0511 | INTEGRATED CIRCUIT, TTL | 01295 | SN7408N | 1 |
| 1820-0615 | INTEGRATED CIRCUIT, TTL | 28480 | 1820-0615 | 1 |
| 1820-1007 | INTEGRATED CIRCUIT | 28480 | 1820-1007 | 3 |
| 1850-0158 | TRANSISTOR, Ge, PNP | 80131 | 2N2635 | 1 |
| 1901-0040 | DIODE, Si, 30 mA, 30 WV | 07263 | FDG1088 | 1 |
| 8159-0005 | JUMPER, wire | 28480 | 8159-0005 | 2 |
| 5040-6001 | EXTRACTOR, PC | 28480 | 5040-6001 | 2 |
| 12539-60003 | TIME BASE GENERATOR | 28480 | 12539-60003 | 1 |
| 12539-90008 | OPERATING AND SERVICE MANUAL | 28480 | 12539-90008 | 1 |

Table 5-2. Code list of Manufacturers

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and the latest supplements.

| Code No. | Manufacturer | Address |
|---|---|---|
| 01295 | Texas Instruments, Inc., Transistor Products Div. | Dallas, Texas |
| 04713 | Motorola, Inc., Semiconductor Prod. Div. | Phoenix, Arizona |
| 07263 | Fairchild Camera & Instr. Corp., Semiconductor Div. | Mountain View, Cal. |
| 28480 | Hewlett-Packard Co. | Palo Alto, Cal. |
| 56289 | Sprague Electric Co. | North Adams, Mass. |
| 72136 | Electro Motive Mfg. Co., Inc. | Willimantic, Conn. |
| 80131 | Electronic Industries Association. Any brand part meeting EIA Standards | Washington, D.C. |


MANUAL PART NO. 12539-90008
MICROFICHE PART NO. 12539-90009

PRINTED IN U.S.A.

'EWLETT
ACKARD DYMEC DIVISION

# DIAGNOSTIC TEST for TIME BASE GENERATOR

model 12539A

MANUAL SUPPLEMENT Aug. 20, 1968

## CONTENTS



This Supplement applies to:

Diagnostic Tape HP 20412B (for HP 2116A/B Computers)
Diagnostic Tape HP 20421A (for HP 2114A/15A Computers)



395 Page Mill Road, Palo Alto, California 94306 Area Code 415 326-1755 TWX 910-373-1296
Europe: 54 Route Des Acacias, Geneva, Switzerland, Cable: "HEWPACKSA" Tel. (022) 42.81.50

Printed in U.S.A.

# DIAGNOSTIC OPERATING PROCEDURE

1. TIME BASE GENERATOR.

2. A Diagnostic Test Tape and Diagnostic Listing is furnished with each Time Base Generator Interface Kit. The HP part number of the tape is on a label attached to the tape and/or container. Use this number and the system serial number for correspondence and re-ordering purposes.

3. This Diagnostic Program checks flag operation, interrupt operation, timing output operation, and relative timing accuracy.

4. PREPARATION.

5. Before using the furnished diagnostic tape, the Teleprinter SIO driver must be added. Use the procedure described in Section II of the Computer Operating Manual. The procedure in brief is:

a. Load and configure the SIO Teleprinter Driver.

b. Load the Diagnostic Test Tape.

NOTE

(If SIO Dump desired)

When using the HP 20421A tape with the HP 2115A/ 14A Computer, insert the following instructions:

1. Set Switch Register to 105, press LOAD ADDRESS.
2. Set Switch Register to 736, press LOAD MEMORY.
3. Continue with 5c.

c. Load the SIO Dump routine.

d. Dump the combined program. (Switch 15 up).

6. OPERATING PROCEDURE.

7. Load the configured tape using the Basic Binary Loader.

8. SEQUENTIAL TEST. After loading the Diagnostic Test tape, test the board using the following procedure:

a. Load the I/O location of the Time Base Generator into the A-Register.

b. Set starting address to 100.

c. Set SWITCH REGISTER to all zeros.

d. Press RUN.

9. The program is now checking the effectiveness of the STF, CLF, SFS, SFC instructions on the Input/Output Control board, and will loop continuously on this test. Assuming no error messages are printed out, set bit 15 of the SWITCH REGISTER to 1 after a few seconds of running time.

10. The message "FT" will be printed out, indicating successful completion of Flag Tests. Set Switch 15 back to 0. The Computer will continue running automatically to the next (Interrupt) test, which can be terminated after a few seconds by setting bit 14 of the SWITCH REGISTER to 1. The message "IN" indicates successful completion of the Interrupt test. Set Switch 14 back to 0.

11. The third test (Operation of timing output) should be allowed to run for 20 minutes. Set bit 13 of the SWITCH REGISTER to 1 as soon as the test is started. The message "OP" indicates successful completion of the Operating test. Set bit 13 back to 0.

12. The fourth test (Timing accuracy) will now be running, and must be allowed to run for about 20 minutes to complete the test. Set bit 12 of the SWITCH REGISTER to 1 as soon as the test is started. The message "TI" indicates successful completion of the Timing accuracy test. Set Switch 12 back to 0. (The program automatically returns to the start of this test as described starting at Paragraph 9. To halt, set bit 6 of the SWITCH REGISTER to 1.

13. INDIVIDUAL TESTS. For purposes of checking and troubleshooting the operation of individual timing outputs, the third test can be looped on any selected time period. Use the same starting procedure as given in Paragraph 8, except in step d set SWITCH REGISTER bit 3 to 1 and set bits 2-1-0 to the desired Time Code as listed in Table 5-1. If so desired, suppress printing by setting bit 5 of the SWITCH REGISTER to 1. The Time Code may be altered during operation.

14. CONTINUOUS TEST. To run the tests for a long period of time (e.g., overnight), leave the SWITCH REGISTER switches (12 through 15) in the "up" position, instead of resetting back to 0, as instructed in Paragraph 9 through 12.

15. REFERENCE INFORMATION.

16. Table 1 lists all messages which may be printed out during the tests, and also lists Switch Register and Halt codes. The following paragraphs describe the meaning of these messages and codes.

17. TEST COMPLETION MESSAGES. A 2-letter completion message is printed on the Teleprinter each time a test exit is manually forced by the appropriate switch. The test may have looped several times (first two tests) or only once (latter two tests). In the sequential mode, the program advances automatically to the next test after exit from the preceding test, and returns to the first after completing the fourth.

18. ERROR MESSAGES. A 2-character error message (EX) is printed out each time an error occurs. The program does not halt. In simplified form, the Flag Tests consist of:

| | | |
|---|---|---|
| 1. | STF 0<br>SFC 0 | Print E0 if not set |
| 2. | SFS 0 | Print E1 if no skip |
| 3. | CLF 0<br>SFS 0 | Print E2 if not clear |
| 4. | SFC 0 | Print E3 if no skip |

19. For Interrupt tests, the program first forces an interrupt by a STC, C (clear flag) to the Time Base Generator and a STF instruction (dummy timing output signal), followed by a STF 0 instruction (interrupt system enable). A properly executed interrupt will skip the E4 message. The second part of the test first turns on the interrupt system (STF 0), starts the Time Base (STC, C), and then lets the 1 ms interval trigger the interrupt. The E5 message is skipped if the interrupt occurs. The third part of the test forces an error condition such that a timing pulse arrives before the Flag is clear from a previous timing pulse. If the Error flip-flop is set, as it should be, the E6 message will be skipped. If an interrupt initiated by these tests arrives too late (during printing of the error message), the program halts and bits 5-0 of the T-Register will be all ones (HLT 77).

20. SWITCH REGISTER SETTINGS. The four most significant bits of the Switch Register are used for exit from the individual tests. Each exit automatically puts the Computer into the next test in sequence, reverting to the first after all four are completed. Bit 6 halts the program whenever desired. Bits 5-0 of the T-Register will contain a code (see Halt Identification) to identify which test the program is in. The test may be resumed by pressing RUN.

21. If a failure occurs and hardware troubleshooting is undertaken, the Switch Register may be used to select the time code. During this time, it may be desirable to suppress repeated printing of the error message, since no further confirmation of a failure is necessary; setting bit 15 to a 1 accomplishes this.

22. HALT IDENTIFICATION. Bits 5-0 of the T-Register will identify the test in progress when the program is halted from the Switch Register (octal codes 01 through 05), or when halted by an erroneous interrupt (octal 77).

Table 1. Diagnostic Reference Information

| | PRINTED MESSAGE | COMMENTS |
|---|---|---|
| TEST COMPLETION MESSAGES | FT | Flag Test successfully completed |
| | IN | Interrupt test successfully completed |
| | OP | Operating test successfully completed |
| | TI | Timing accuracy test successfully completed |
| ERROR MESSAGES | E0 | Flag test, Set Flag failed |
| | E1 | Flag test, Skip Flag Set failed |
| | E2 | Flag test, Clear Flag failed |
| | E3 | Flag test, Skip Flag Clear failed |
| | E4 | Interrupt test, forced interrupt failed |
| | E5 | Interrupt test, Flag interrupt failed |
| | E6 | Interrupt test, Timing Error circuit failed |
| | EA | Operation test, .1 ms failed |
| | EB | Operation test, 1 ms failed |
| | EC | Operation test, 10 ms failed |
| | ED | Operation test, 100 ms failed |
| | EE | Operation test, 1 sec failed |
| | EF | Operation test, 10 sec failed |
| | EG | Operation test, 100 sec failed |
| | EH | Operation test, 1000 sec failed |
| | E7 | Timing test, no interrupt |
| | E8 | Timing test, time short |
| | E9 | Timing test, time long |

Table 1. (Cont'd)

| | BITS | SETTING | FUNCTION |
|---|---|---|---|
| SWITCH REGISTER SETTINGS | 15 | 1 | Exit Flag Test |
| | 14 | 1 | Exit Interrupt test |
| | 13 | 1 | Exit Operation test |
| | 12 | 1 | Exit Timing Accuracy test |
| | 6 | 1 | Halt |
| | 5 | 0 | Print messages on Teleprinter |
| | 5 | 1 | Suppress printing |
| | 3 | 0 | Use sequential Time Codes |
| | 3 | 1 | Use Switches 2-1-0 to enter Time Code |
| | 2-1-0 | 000 | .1 ms Time Code |
| | | 001 | 1 ms Time Code |
| | | 010 | 10 ms Time Code |
| | | 011 | 100 ms Time Code |
| | | 100 | 1 sec Time Code |
| | | 101 | 10 sec Time Code |
| | | 110 | 100 sec Time Code |
| | | 111 | 1000 sec Time Code |
| | T-REGISTER BITS 5-0 (OCTAL) | | |
| HALT IDENTIFICATION | 01 | | Flag Test |
| | 02 | | Interrupt test |
| | 03 | | Operation (sequential) test |
| | 04 | | Operation (individual) test |
| | 05 | | Timing accuracy test |
| | 77 | | Error Interrupt |

# 2115A TIME BASE

# GENERATOR TEST

Binary Tape - HP20421A

Source Listing- HP20421AL

0001 ASMB,A,B,L,T MARCH 8, 1968

| | |
|---|---|
| TBG | 000166 |
| C1 | 000167 |
| C2 | 000170 |
| C3 | 000171 |
| C4 | 000172 |
| C5 | 000173 |
| C6 | 000174 |
| C7 | 000175 |
| C9 | 000176 |
| FTR | 000177 |
| FT1 | 000200 |
| FT2 | 000201 |
| FT3 | 000205 |
| FT4 | 000207 |
| FT5 | 000210 |
| FT6 | 000214 |
| FT7 | 000223 |
| ER1 | 000231 |
| ER2 | 000234 |
| INTR | 000237 |
| INTA | 000241 |
| INTB | 000242 |
| INS | 000250 |
| INTC | 000255 |
| INTD | 000257 |
| INT | 000263 |
| INTE | 000266 |
| INTF | 000267 |
| INTH | 000270 |
| INTK | 000275 |
| INTJ | 000303 |
| INTG | 000311 |
| INTI | 000317 |
| INTL | 000321 |
| AB | 000325 |
| CNTI | 000326 |
| NTST | 000327 |
| AJSB | 000345 |
| EINTR | 000346 |
| EIN | 000354 |
| IM1 | 000355 |
| AJMP | 000356 |
| BJMP | 000357 |
| OPR | 000360 |
| OPR1 | 000371 |
| OPR2 | 000372 |
| OPR3 | 000374 |
| ENDCK | 000405 |
| SAR | 000422 |
| OPR4 | 000427 |
| OPR5 | 000431 |
| ENDCL | 000442 |
| EXIT | 000451 |
| STOP1 | 000456 |
| STOP2 | 000460 |
| ERROP | 000462 |

```
NEXT     000472
PLUSR    000502
CJMP     000505
DJMP     000506
TCD      000507
TCE      000510
EROP     000511
MSK1     000512
LONGT    000513
LONG1    000522
LONG2    000524
LONGX    000525
LONGY    000533
LONGZ    000547
CNTR1    000565
CNTR2    000566
CONST    000567
XHI      000570
XLO      000571
EJMP     000572
ER3      000573
ER4      000576
ER5      000601
FT       000604
IN       000606
OP       000610
TI       000612
E0       000614
E1       000616
E2       000620
E3       000622
E4       000624
E5       000626
E6       000630
E7       000632
E8       000634
E9       000636
TIMER    000640
EA       000641
EB       000642
EC       000643
ED       000644
EE       000645
EF       000646
EG       000647
EH       000650
WAIT     000651
WAIT1    000663
WAIT2    000672
WAIT3    000701
WAIT4    000706
WAIT5    000707
WAIT6    000714
TM2      000715
OT2      000716
TMP1     000733
TMP2     000734
```

```
ML       000735
**   NO ERRORS*
```

```
0001                ASMB,A,B,L,T        MARCH 8, 1968
0002*
0003*
0004*                   TIME BASE GENERATOR TEST (2115A)
0005*
0006*    THIS TEST EXERCISES THE HP 12539A TIME BASE GENERATOR
0007*    INTERFACE BD.
0008*
0009*    LOAD TIME BASE GENERATOR (TBG) I/O LOCATION INTO "A"
0010*
0011*    STARTING ADDRESS = 1008
0012*
0013*    ************************************************************
0014*    *                                                          *
0015*    *    TEST COMPLETION SIGNS AND ERROR REPORTS               *
0016*    *                                                          *
0017*    *    FT   INDICATES FLAG TEST COMPLETED.                   *
0018*    *    IN   INDICATES INTERRUPT TEST COMPLETED.              *
0019*    *    OP   INDICATES OPERATING TEST COMPLETED.              *
0020*    *    TI   INDICATES TIMING TEST COMPLETED                  *
0021*    *                                                          *
0022*    *    ERRORS                                                *
0023*    *                                                          *
0024*    *                                                          *
0025*    *    E0 = FLAG TEST. SET FLAG FAILED.                      *
0026*    *    E1 = FLAG TEST. SKIP FLAG SET FAILED.                 *
0027*    *    E2 = FLAG TEST. CLEAR FLAG FAILED.                    *
0028*    *    E3 = FLAG TEST. SKIP CLEAR FLAG FAILED.               *
0029*    *                                                          *
0030*    *    E4 = INTERRUPT TEST. FORCED INTERRUPT FAILED.         *
0031*    *    E5 = INTERRUPT TEST. FLAG INTERRUPT FAILED.           *
0032*    *    E6 = INTERRUPT TEST. TIMING ERROR CKT FAILED.         *
0033*    *                                                          *
0034*    *                                                          *
0035*    *    EA = OPERATION TEST.  .1MS FAILED.        0 BIT     *
0036*    *    EB = OPERATION TEST.   1MS FAILED.        1         *
0037*    *    EC = OPERATION TEST.   10MS FAILED.       2         *
0038*    *    ED = OPERATION TEST.   100MS FAILED.      3         *
0039*    *    EE = OPERATION TEST.   1 SEC FAILED.      4         *
0040*    *    EF = OPERATION TEST.   10 SEC FAILED.     5         *
0041*    *    EG = OPERATION TEST.   100 SEC FAILED.    6         *
0042*    *    EH = OPERATION TEST.   1000 SEC FAILED.   7 BIT     *
0043*    *                                                          *
0044*    *    E7   TIMING TEST.   NO INTERRUPT.                     *
0045*    *    E8   TIMING TEST.   TIME SHORT.                       *
0046*    *    E9   TIMING TEST.   TIME LONG.                        *
0047*    *                                                          *
0048*    ************************************************************
0049*
0050*
0051*
0052*
0053*
0054*
0055*    SWITCH SETTINGS
0056*
0057*    SW 0-2     TIME CODE
```

```
0058*
0059*     SW3 = 0    USE SEQUENTIAL TIME CODE
0060*     SW3 = 1    USE SW 0-2  TO ENTER TIME CODE
0061*
0062*     SW5 = 0    PRINT DIAGNOSTICS ON TTY.
0063*     SW5 = 1    SUPPRESS PRINT.
0064*
0065*     SW6 = 1    HALT.
0066*
0067*
0068*     ROUTINES WILL LOOP TO THEIR STARTING POINT UNTIL EXIT SWITCH
0069*     IS SENSED.
0070*
0071*     SW15 = 1   EXIT FLAG TEST.
0072*
0073*     SW14 = 1   EXIT INTERRUPT TEST
0074*
0075*     SW13 = 1   EXIT OPERATION TEST
0076*                COMPLETE TEST ABOUT 18 MIN.
0077*
0078*     SW12 = 1   EXIT TIMING TEST
0079*                COMPLETE TEST ABOUT 16 2/3 MIN.
0080*
0081*
0082*
0083  00100                ORG 100B
0084  00100 024110         JMP 110B
0085  00110                ORG 110B
0086  00110 070166         STA TBG        STORE ADDRESS OF TIME BASE.
0087*
0088*
0089*
0090*     THIS SECTION SETS UP I/O INSTRUCTIONS WITH ADDRESS FROM
0091*     SWITCH SETTINGS AT START OF THIS ROUTINE.
0092*
0093*
0094  00111 060167         LDA C1         SET UP STF 0.
0095  00112 030166         IOR TBG        ADD I/O LOCATION
0096  00113 070200         STA FT1        FLAG TEST
0097  00114 070242         STA INTB       INTERRUPT TEST
0098*
0099  00115 060170         LDA C2         SET UP CLF 0.
0100  00116 030166         IOR TBG        ADD I/O LOCATION
0101  00117 070207         STA FT4        FLAG TEST
0102*
0103  00120 060171         LDA C3         SET UP SFC 0
0104  00121 030166         IOR TBG        ADD I/O LOCATION
0105  00122 070201         STA FT2        FLAG TEST
0106  00123 070214         STA FT6          "
0107  00124 070275         STA INTK       ERROR CKT TEST
0108*
0109  00125 060172         LDA C4         SET UP SFS 0
0110  00126 030166         IOR TBG        ADD I/O LOCATION.
0111  00127 070205         STA FT3        FLAG TEST.
0112  00130 070210         STA FT5          "
0113*
0114  00131 060173         LDA C5         SET UP STC 0,C
```

```
0115  00132 030166          IOR TBG         ADD I/O LOCATION
0116  00133 070241          STA INTA        INTERRUPT TEST
0117  00134 070257          STA INTD
0118  00135 070267          STA INTF
0119  00136 070317          STA INTI
0120  00137 070374          STA OPR3        OPERATION TEST
0121  00140 070431          STA OPR5
0122  00141 070524          STA LONG2       TIMING TEST
0123*
0124  00142 060174          LDA C6          SET UP OTA 0
0125  00143 030166          IOR TBG         ADD I/O LOCATION
0126  00144 070255          STA INTC        INTERRUPT TEST
0127  00145 070266          STA INTE
0128  00146 070372          STA OPR2        OPERATION TEST
0129  00147 070427          STA OPR4
0130  00150 070522          STA LONG1       TIMING TEST
0131*
0132  00151 060175          LDA C7          SET UP LIB 0
0133  00152 030166          IOR TBG         ADD TBG ADDRESS
0134  00153 070303          STA INTJ
0135  00154 070321          STA INTL
0136*
0137*
0138  00155 060176          LDA C9          SET UP LIA 0
0139  00156 030166          IOR TBG         ADD TBG ADDRESS
0140  00157 070311          STA INTG
0141  00160 070270          STA INTH
0142  00161 070303          STA INTJ
0143  00162 070321          STA INTL
0144  00163 060345          LDA AJSB        SET UP INTERRUPT ERROR
0145  00164 170166          STA TBG,I       AJSB = JSB EINTR
0146*
0147  00165 024177          JMP FTR
0148*
0149  00166 000000  TBG     NOP             I/O LOCATION
0150*
0151*    I/O INSTRUCTIONS
0152*
0153  00167 102100  C1      STF 0           SET FLAG
0154  00170 103100  C2      CLF 0           CLEAR FLAG
0155  00171 102200  C3      SFC 0           SKIP FLAG CLEAR
0156  00172 102300  C4      SFS 0           SKIP FLAG SET.
0157  00173 103700  C5      STC 0,C         SET CONTROL BIT, CLEAR FLAG
0158  00174 102600  C6      OTA 0           OUTPUT "A"
0159  00175 106500  C7      LIB 0           INPUT TO B
0160  00176 102500  C9      LIA 0           INPUT TO A
0161*
0162*
0163*
0164*
0165*                       FLAG TEST ROUTINE
0166*
0167*     THIS SECTION TEST "SET FLAG","CLEAR FLAG"
0168*     "SKIP SET FLAG", AND "SKIP CLEAR FLAG" INSTRUCTIONS.
0169*
0170*     THE ROUTINE WILL LOOP IN THIS TEST UNTIL SW 15 IS SET.
0171*     IT WILL THEN EXIT TO THE INTESRUPT SECTION.
```

```
0172*
0173*     SW 15 = 1 EXIT THIS TEST.
0174*
0175*
0176   00177 107700  FTR    CLC 0,C         INTERRUPT SYSTEM OFF
0177   00200 102100  FT1    STF 0           SET TBG FLAG
0178   00201 102200  FT2    SFC 0           IF FLAG IS CLEAR PRINT ERROR.
0179   00202 024205         JMP *+3         FLAG SET OK.
0180   00203 064614         LDB E0          FLAG NOT SET. STF FAILED.
0181   00204 014716         JSB OT2         PRINT ERROR.
0182*
0183*
0184   00205 102300  FT3    SFS 0           SKIP ON SET FLAG.
0185   00206 024231         JMP ER1         SKIP INSTRUCTION FAILED.
0186*
0187*
0188   00207 103100  FT4    CLF 0           CLEAR FLAG.
0189   00210 102300  FT5    SFS 0           SKIP IF FLAG STILL SET.
0190   00211 024214         JMP *+3         FLAG IS CLEAR. OK.
0191   00212 064620         LDB E2          SHOULD NOT HAVE SKIPPED
0192   00213 014716         JSB OT2         PRINT ERROR.
0193   00214 102200  FT6    SFC 0           SKIP IF FLAG CLEARED
0194   00215 024234         JMP ER2         ERROR. SHOULD HAVE SKIPPED.
0195*
0196*     CHECK FOR EXIT OR HLT INSTRUCTION.
0197*
0198   00216 102501         LIA 01          CHECK FOR HALT
0199   00217 001727         ALF,ALF
0200   00220 001200         RAL             ROTATE BIT 6
0201   00221 002020         SSA
0202   00222 102001         HLT 01B         SET HALT
0203   00223 102501  FT7    LIA 01          NOT SET.CHECK SW 15
0204   00224 002021         SSA,RSS
0205   00225 024200         JMP FT1         NOT SET. LOOP THIS TEST AGAIN.
0206   00226 064604         LDB FT          SW15 SET. TYPE OUT "FT" AND
0207   00227 014716         JSB OT2         CONTINUE WITH NEXT TEST.
0208   00230 024237         JMP INTR        GO TO INTERRUPT TEST.
0209*
0210*     ERROR MESSAGE ROUTINES.
0211*
0212   00231 064616  ER1    LDB E1          LOAD ASCII FOR MESSAGE.
0213   00232 014716         JSB OT2         PRINT IT
0214   00233 024207         JMP FT4         CONTINUE WITH NEXT PART OF TEST.
0215*
0216*
0217   00234 064622  ER2    LDB E3          LOAD ASCII FOR MESSAGE.
0218   00235 014716         JSB OT2         PRINT IT
0219   00236 024223         JMP FT7         CHECK FOR EXIT INSTRUCTION.
0220*
0221*
0222*
0223*
0224*
0225*                    INTERRUPT TEST
0226*
0227*     THE FIRST SECTION OF THIS TEST FORCES AN INTERRUPT
0228*     BY STC TBG AND AN STF 0 INSTRUCTION, THE NEXT SECTION
```

```
0229*     WILL ALLOW THE TBG TO CAUSE AN INTERRUPT.
0230*
0231*     FAILURE TO CAUSE AN INTERRUPT IN THIS FIRST SECTION
0232*     WILL CAUSE AN "E4" TO BE TYPED OUT.
0233*
0234*     THE ROUTINE WILL LOOP IN THIS TEST UNTIL SW 14 IS SET.
0235*     IT WILL THEN EXIT TO THE OPERATION TEST.
0236*
0237*     SW14 = 1  EXIT TO NEXT TEST.
0238*
0239*
0240*
0241   00237 060356   INTR   LDA AJMP        SET UP INTERRUPT INSTRUCTIONS.
0242   00240 170166          STA TBG,I       AJMP= JMP INS
0243   00241 103700   INTA   STC 0,C        SET CONTROL TBG
0244   00242 102100   INTB   STF 0          SET TBG FLAG
0245   00243 102100          STF 0          INTERRUPT ON.
0246   00244 000000          NOP            MARK TIME
0247   00245 000000          NOP
0248   00246 064624          LDB E4         SHOULD SKIP THIS
0249   00247 014716          JSB OT2        OUTPUT ERROR MESSAGE
0250   00250 103100   INS    CLF 0          INTERRUPT SYSTEM OFF
0251   00251 106700          CLC 0
0252*
0253*
0254   00252 060357          LDA BJMP       SET UP INTERRUPT INSTRUCTION
0255   00253 170166          STA TBG,I      BJMP = JMP INT
0256   00254 060355          LDA TM1        1MS. INSTRUCTION
0257   00255 102600   INTC   OTA 0          OUTPUT INSTRUCTION
0258   00256 102100          STF 0          INTERRUPT SYSTEM ON.
0259   00257 103700   INTD   STC 0,C        START TBG.
0260   00260 014651          JSB WAIT       LONG WAIT.
0261   00261 064526          LDB E5         SHOULD SKIP THIS.
0262   00262 014716          JSB OT2        OUTPUT ERROR MESSAGE.
0263   00263 103100   INT    CLF 0          INTERRUPT SYSTEM OFF.
0264   00264 106700          CLC 0
0265*
0266*
0267*     ERROR CKT TEST
0268*
0269   00265 002400          CLA
0270   00266 102600   INTE   OTA 0          OUTPUT 100 USEC
0271   00267 103700   INTF   STC 0,C        START COUNT - CLEAR FLAG
0272   00270 102500   INTH   LIA 0          GET STATUS
0273   00271 064630          LDB E6
0274   00272 002002          SZA            CHECK FOR NO ERROR
0275   00273 014716          JSB OT2
0276   00274 002400          CLA
0277   00275 102200   INTK   SFC 0          WAIT FOR FLAG
0278   00276 024302          JMP *+4        FLAG SET!
0279   00277 002004          INA
0280   00300 002002          SZA
0281   00301 024275          JMP *-4
0282   00302 064630          LDB E6
0283   00303 102500   INTJ   LIA 0          GET STATUS
0284   00304 002002          SZA            CHECK FOR NO ERROR
0285   00305 014716          JSB OT2
```

```
0286  00306 064326          LDB CNTI        GET COUNTER
0287  00307 006006          INB,SZB         DELAY TO FORCE ERROR
0288  00310 024307          JMP *-1
0289  00311 102500  INTG    LIA 0           GET STATUS
0290  00312 010325          AND AB          MASK OCT 20
0291  00313 002002          SZA             CHECK FOR ERROR
0292  00314 024317          JMP *+3
0293  00315 064530          LDB E6
0294  00316 014716          JSB OT2
0295  00317 103700  INTI    STC 0,C         CLEAR ERROR
0296  00320 064630          LDB E6
0297  00321 102500  INTL    LIA 0           GET STATUS
0298  00322 002002          SZA             CHECK FOR NO ERROR
0299  00323 014716          JSB OT2
0300  00324 024327          JMP NTST
0301*
0302  00325 000020  AB      OCT 20
0303  00326 177740  CNTI    OCT 177740
0304*
0305*
0306*     EXIT CHECK
0307*
0308  00327 060345  NTST    LDA AJSB        ERROR INTERRUPT INSTRUCTION
0309  00330 173166          STA T8G,I       AJSB= JSB EINTR
0310*
0311  00331 102501          LIA 01          CHECK FOR HALT SWITCH
0312  00332 001727          ALF,ALF
0313  00333 001200          RAL             ROTATE BIT 6
0314  00334 002020          SSA
0315  00335 102002          HLT 02B         BIT 6 SET, HALT.
0316*
0317  00336 102501          LIA 01          CHECK FOR EXIT SW 14
0318  00337 001200          RAL             ROTATE
0319  00340 002021          SSA,RSS
0320  00341 024237          JMP INTR        NOT SET, LOOP THIS TEST.
0321  00342 064606          LDB IN          SW14 SET, TYPE OUT "IN" AND
0322  00343 014716          JSB OT2         CONTINUE WITH NEXT TEST
0323  00344 024360          JMP OPR         GO TO OPERATING TEST.
0324*
0325*
0326  00345 014346  AJSB    JSB EINTR       ERROR INTERRUPT INSTRUCTION
0327*
0328*     ERROR INTERRUPT ROUTINE.
0329*
0330*     "A" REGISTER IS SAVED
0331*     "B" REGISTER CONTAINS ADDRESS WHEN INTERRUPT OCCURS.
0332*
0333  00346 000000  EINTR   NOP
0334  00347 074354          STB EIN         SAVE "B" REGISTER.
0335  00350 064346          LDB EINTR       LOAD INTERRUPT ADDRESS.
0336  00351 102077          HLT 77B
0337  00352 064354          LDB EIN         RESTORE "B" REGISTER.
0338  00353 124346          JMP EINTR,I     RETURN
0339*
0340*
0341  00354 000000  EIN     NOP             STORAGE FOR "B" REGISTER
0342  00355 000001  TM1     OCT 1           1 MS. TIME CODE.
```

```
0343*
0344   00356 024250   AJMP   JMP INS        INTERRUPT JUMP INSTRUCTION
0345   00357 024263   BJMP   JMP INT        SAME
0346*
0347*
0348*
0349*
0350*
0351*                      OPERATION TEST
0352*
0353*     THIS SECTION TESTS 7 BITS WHICH CONTROL THE INTERRUPT TIMES.
0354*
0355*     TWO PATTERNS ARE AVAILABLE.  IF SW 3 IS SET, SW 0-2 ARE USED
0356*     TO ENTER THE TIME CODE DESIRED. IF SW 3 IS CLEAR A SEQUENTIAL
0357*     PATTERN, TESTING ALL CODE BITS, WILL BE USED.
0358*
0359*     THE ENTIRE SECTION TAKES ABOUT 18 MIN.
0360*
0361*
0362*     ENTER WITH SW 3 SET AS DESIRED.
0363*
0364*     SW SETTINGS
0365*
0366*     SW 0-2     SET TIME CODE
0367*
0368*     SW3 = 0    USE SEQUENTIAL PATTERN
0369*     SW3 = 1    USE SW 0-2 FOR TIME CODE
0370*
0371*     SW6 = 1    HALT 38
0372*
0373*     SW13 = 0   LOOP THIS TEST.
0374*     SW13 = 1   EXIT.
0375*
0376*
0377*     ERRORS ARE "EA" TO "EH". CHECK START OF TEST FOR DEFINITION.
0378*
0379*
0380   00360 102501   OPR    LIA 01          CHECK SW 3 FOR PATTERN.
0381   00361 001323          RAR,RAR
0382   00362 001300          RAR             RIGHT 3.
0383   00363 000010          SLA
0384   00364 024422          JMP SWR         SW3 SET USE SWITCHES TO LOAD
0385   00365 002400          CLA             NOT SET.
0386   00366 070507          STA TCD         CLEAR TIME CODE STORAGE
0387   00367 060505          LDA CJMP        SET INTERRUPT INSTRUCTION.
0388   00370 170166          STA TBG,I       CJMP = JMP ENDCK
0389   00371 060507   OPR1   LDA TCD         GET TIME CODE.
0390   00372 102600   OPR2   OTA 0           OUTPUT CODE
0391   00373 102100          STF 0           INTERRUPT SYSTEM ON.
0392   00374 103700   OPR3   STC 0,C         SET CONTROL AND START TBG.
0393   00375 102501          LIA 01          CHECK FOR HALT
0394   00376 001727          ALF,ALF         SW 6 SET?
0395   00377 001200          RAL
0396   00400 002020          SSA
0397   00401 024456          JMP STOP1       YES, GO TO 1ST HALT ROUTINE.
0398*
0399*
```

```
0400*
0401   00402 014651          JSB WAIT        LONG WAIT
0402   00403 000000          NOP
0403   00404 014462          JSB ERROP       ERROR SHOULD HAVE SKIPPED THIS.
0404*
0405*
0406   00405 103100  ENDCK    CLF 0
0407   00406 106700          CLC 0           INTERRUPT SYSTEM OFF.
0408   00407 060507          LDA TCD         CHECK FOR LAST TIME CODE.
0409   00410 010512          AND MSK1        OCT 7 STRIP EXCESS.
0410   00411 050512          CPA MSK1
0411   00412 024415          JMP *+3         YES
0412   00413 034507          ISZ TCD         NO. INCREASE AND GET NEXT CODE.
0413   00414 024371          JMP OPR1
0414*
0415   00415 102501          LIA 01          CHECK FOR EXIT.
0416   00416 001222          RAL,RAL         SW 13 SET?
0417   00417 002021          SSA,RSS
0418   00420 024360          JMP OPR         NOT SET. LOOP AGAIN.
0419   00421 024451          JMP EXIT        YES, LEAVE THIS ROUTINE
0420*
0421*
0422*
0423*     THIS SECTION USES THE SW TO ENTER TIME CODE
0424*
0425   00422 102501  SWR     LIA 01          LOAD SW.
0426   00423 070507          STA TCD         TIME CODE STORAGE
0427   00424 060506          LDA DJMP        SET INTERRUPT INSTRUCTIONS
0428   00425 170166          STA TBG,I       DJMP= JMP ENDCL
0429   00426 060507          LDA TCD         GET THE TIME CODE.
0430   00427 102600  OPR4    OTA 0           OUTPUT THE CODE
0431   00430 102100          STF 0           INTERRUPT SYSTEM ON.
0432   00431 103700  OPR5    STC 0,C         SET CONTROL AND START TBG.
0433*
0434*
0435   00432 102501          LIA 01          CHECK FOR HALT
0436   00433 001727          ALF,ALF         SW 6 SET
0437   00434 001200          RAL
0438   00435 002020          SSA
0439   00436 024460          JMP STOP2       YES. GO TO 2ND HALT ROUTINE.
0440*
0441*
0442*
0443   00437 014651          JSB WAIT        LONG WAIT
0444   00440 000000          NOP
0445   00441 014462          JSB ERROP       ERROR SHOULD HAVE SKIPPED THIS.
0446*
0447*
0448   00442 103100  ENDCL    CLF 0           INTERRUPT SYSTEM OFF
0449   00443 106700          CLC 0
0450   00444 102501          LIA 01          CHECK FOR EXIT
0451   00445 001222          RAL,RAL
0452   00446 002021          SSA,RSS         SW 13 SET
0453   00447 024360          JMP OPR         NO. LOOP AGAIN
0454   00450 024451          JMP EXIT        YES.
0455*
0456*
```

```
0457   00451 060345  EXIT  LDA AJSB       RESTORE ERROR INTRP.INST.
0458   00452 170166        STA TBG,I      AJSB= JSB EINTR
0459   00453 064610        LDB OP         LOAD "OP" ASCII
0460   00454 014716        JSB OT2
0461   00455 024513        JMP LONGT      GO TO TIMING ROUTINE
0462*
0463*
0464*
0465   00456 102003  STOP1 HLT 03
0466   00457 024405        JMP ENDCK      CHECK END CODE.
0467*
0468*
0469   00460 102004  STOP2 HLT 04
0470   00461 024442        JMP ENDCL      CHECK SW.
0471*
0472*
0473*     ERROR ROUTINES
0474*
0475*     NO ENTRY REQUIREMENTS.
0476*
0477   00462 000000  ERROP NOP
0478   00463 103100        CLF 0          INTERRUPT SYSTEM OFF.
0479   00464 106700        CLC 0
0480   00465 060540        LDA TIMER      SET UP MESSAGE TABLE
0481   00466 070511        STA EROP       SAVE IN WORKING STORAGE
0482   00467 034511        ISZ EROP       INCREMENT FOR FIRST ADDRESS
0483   00470 002400        CLA
0484   00471 070510        STA TCE        CLEAR WORKING REGISTER
0485   00472 060507  NEXT  LDA TCD        GET TIME CODE
0486   00473 010512        AND MSK1       CLEAR OFF EXCESS.
0487   00474 050510        CPA TCE        COMPARE WITH WORKING REGISTER.
0488   00475 024477        JMP *+2        GOOD MATCH.
0489   00476 024502        JMP PLUSR      NO MATCH. TRY NEXT ONE.
0490   00477 064511        LDB EROP       GOOD. LOAD FROM THIS ADDRESS.
0491   00500 014716        JSB OT2        PRINT ASCII MESSAGE.
0492   00501 124462        JMP ERROP,I    EXIT.
0493*
0494   00502 034510  PLUSR ISZ TCE        INCREMENT WORKING REGISTER
0495   00503 034511        ISZ EROP       INCREMENT MESSAGE TABLE.
0496   00504 024472        JMP NEXT       TRY AGAIN.
0497*
0498*
0499*     CONSTANTS AND STORAGE
0500*
0501*
0502   00505 024405  CJMP  JMP ENDCK      INTERRUPT INSTRUCTIONS
0503   00506 024442  DJMP  JMP ENDCL        "
0504*
0505*
0506   00507 000000  TCD   NOP            WORKING REGISTERS
0507   00510 000000  TCE   NOP              "
0508   00511 000000  EROP  NOP              "
0509   00512 000007  MSK1  OCT 7          MASK
0510*
0511*
0512*
0513*
```

```
0514*                          TIMING TEST
0515*
0516*       THIS TEST IS TO DETECT A "GROSS" TIMING ERROR. IT USES
0517*       ALL OF THE DECADE DIVIDERS ON THE TIME BASE BOARD IN
0518*       CASCADE AND ALLOWS PLUS OR MINUS 1 PCT TIMING DIFFERENCE
0519*       BETWEEN THE COMPUTER BASIC CLOCK AND THE TBG.  TO OBTAIN
0520*       THE ACCURACY COMENSURATE WITH THAT OF THE 100 KC CRYSTAL
0521*       USED ON THE TBG, USE AN EXTERNAL ACCURATE FREQUENCY/TIME
0522*       INTERVAL METER ON TEST POINT 1
0523*
0524*
0525*       ERRORS
0526*
0527*       E7    NO INTERRUPT DURING TIMING GAP
0528*       E8    TIME SHORT
0529*       E9    TIME LONG.
0530*
0531*       SW SETTINGS
0532*
0533*       SW12 = 0  LOOP THIS TEST
0534*       SW12 = 1  EXIT TO FLAG TEST
0535*
0536*       SW6 = 1   HALT 5B
0537*
0538*
0539*
0540  00513 060572  LONGT LDA EJMP       SET INTERRUPT INSTRUCTION
0541  00514 170166        STA TBG,I      EJMP = JMP LONGY
0542  00515 002400        CLA
0543  00516 070565        STA CNTR1      CLEAR WORKING COUNTERS
0544  00517 060567        LDA CONST
0545  00520 070566        STA CNTR2
0546  00521 060512        LDA MSK1       GET TIME CODE FOR 1000 SEC.
0547  00522 102600  LONG1 OTA 0          OUTPUT TIME CODE
0548  00523 102100        STF 0          TURN INTERRUPT ON.
0549  00524 103700  LONG2 STC 0,C       START THE CLOCK
0550  00525 034565  LONGX ISZ CNTR1     INCREMENT CLOCK TIMER
0551  00526 024525        JMP *-1
0552  00527 034566        ISZ CNTR2      CONTINUE COUNTING
0553  00530 024525        JMP LONGX
0554  00531 064632        LDB E7         ERROR. SHOULD SKIP THIS
0555  00532 014716        JSB OT2        PRINT ERROR MESSAGE
0556*
0557*
0558  00533 103100  LONGY CLF 0
0559  00534 106700        CLC 0          TURN INTERRUPT OFF
0560*
0561*
0562  00535 060566        LDA CNTR2      CHECK LARGE COUNTER
0563  00536 002021        SSA,RSS
0564  00537 024573        JMP ER3        ERROR
0565*
0566*
0567*
0568  00540 040570        ADA XHI        SUBTRACT FROM UPPER LIMIT
0569  00541 002021        SSA,RSS
0570  00542 024576        JMP ER4        ERROR. CLOCK SLOW
```

```
0571*
0572*
0573*
0574  00543 060566          LDA CNTR2     GET COUNTER AGAIN
0575  00544 040571          ADA XLO       SUBTRACT FROM LOWER LIMIT
0576  00545 002020          SSA
0577  00546 024601          JMP ER5       ERROR CLOCK FAST
0578*
0579*
0580*
0581  00547 102501  LONGZ    LIA 01        CHECK SW 6 FOR HALT
0582  00550 001727          ALF,ALF
0583  00551 001200          RAL
0584  00552 002020          SSA           SW 6 SET?
0585  00553 102005          HLT 05B       YES
0586*
0587*
0588*
0589  00554 102501          LIA 01        NO. CHECK FOR EXIT.
0590  00555 001723          ALF,RAR
0591  00556 002021          SSA,RSS       SW12 SET?
0592  00557 024513          JMP LONGT     NO. LOOP THIS TEST.
0593*
0594*
0595*
0596  00560 064512          LDB TI        YES GET TEXT
0597  00561 014716          JSB OT2       PRINT IT
0598*
0599*
0600*
0601  00562 060345          LDA AJSB      RESET ERROR INTERRUPT
0602  00563 170166          STA TBG,I     AJSB - JSB EINTR.
0603  00564 024200          JMP FT1       EXIT TO FLAG TEST AGAIN.
0604*
0605*
0606*
0607  00565 000000  CNTR1    NOP           CLOCK COUNTERS
0608  00566 000000  CNTR2    NOP
0609  00567 172777  CONST    OCT 172777
0610  00570 000275  XHI      OCT 275       UPPER LIMIT
0611  00571 000354  XLO      OCT 354       LOWER LIMIT
0612*
0613  00572 024533  EJMP     JMP LONGY     INTERRUPT INSTRUCTION.
0614*
0615*
0616  00573 064632  ER3      LDB E7        LOAD ERROR      NO INTERRUPT
0617  00574 014716           JSB OT2       PRINT
0618  00575 024547           JMP LONGZ     CHECK FOR EXIT
0619*
0620  00576 064636  ER4      LDB E9        LOAD ERROR.     CLOCK SLOW.
0621  00577 014716           JSB OT2       PRINT
0622  00600 024547           JMP LONGZ     CHECK FOR EXIT
0623*
0624  00601 064634  ER5      LDB E8        LOAD ERROR.     CLOCK FAST.
0625  00602 014716           JSB OT2       PRINT
0626  00603 024547           JMP LONGZ     CHECK FOR EXIT.
0627*
```

```
0628*    MESSAGES.
0629*
0630  00604 000605  FT    DEF *+1       FLAG TEST COMPLETED
0631  00605 043124        ASC 1,FT
0632  00606 000607  IN    DEF *+1       INTERRUPT TEST COMPLETED
0633  00607 044516        ASC 1,IN
0634  00610 000611  OP    DEF *+1       OPERATION TEST COMPLETED
0635  00611 047520        ASC 1,OP
0636  00612 000613  TI    DEF *+1       TIMING TEST COMPLETED
0637  00613 052111        ASC 1,TI
0638*
0639*
0640*    ERROR DIAGNOSTICS.
0641*
0642*
0643  00614 000615  E0    DEF *+1       ERROR, SET FAG FAILED
0644  00615 042460        ASC 1,E0
0645  00616 000617  E1    DEF *+1         "    SKIP SET FLAG FAILED
0646  00617 042461        ASC 1,E1
0647  00620 000621  E2    DEF *+1         "    CLEAR FLAG FAILED
0648  00621 042462        ASC 1,E2
0649  00622 000623  E3    DEF *+1         "    SKIP CLEAR FLAG FAILED
0650  00623 042463        ASC 1,E3
0651  00624 000625  E4    DEF *+1         "    FORCED INTERRUPT FAILED
0652  00625 042464        ASC 1,E4
0653  00626 000627  E5    DEF *+1         "    FLAG INTERRUPT FAILED
0654  00627 042465        ASC 1,E5
0655  00630 000631  E6    DEF *+1         "    INTERRUPT GATE FAILED
0656  00631 042466        ASC 1,E6
0657  00632 000633  E7    DEF *+1         "    NO INTERRUPT - DECADE FAIL
0658  00633 042467        ASC 1,E7
0659  00634 000635  E8    DEF *+1         "    TIME SHORT - CLOCK FAST
0660  00635 042470        ASC 1,E8
0661  00636 000637  E9    DEF *+1         "    TIME LONG = CLOCK SLOW
0662  00637 042471        ASC 1,E9
0663*
0664*
0665*
0666  00640 000640  TIMER DEF *
0667  00641 042501  EA    ASC 1,EA       ERROR  .1MS    FAILED
0668  00642 042502  EB    ASC 1,EB         "    1MS      "
0669  00643 042503  EC    ASC 1,EC         "    10MS     "
0670  00644 042504  ED    ASC 1,ED         "    100MS    "
0671  00645 042505  EE    ASC 1,EE         "    1 SEC    "
0672  00646 042506  EF    ASC 1,EF         "    10 SEC   "
0673  00647 042507  EG    ASC 1,EG         "    100 SEC  "
0674  00650 042510  EH    ASC 1,EH         "    1000 SEC "
0675*
0676*
0677*
0678*
0679*                    SERVICE SUBROUTINES
0680*
0681*
0682*
0683*                    DELAY GENERATOR
0684*
```

```
0685*     ENTER WITH TIME CODE STORED IN TCD. ACCUMULATORS NOT SAVED.
0686*
0687*      MINIMUM DELAY IS 340MS.
0688*
0689*     TIME CODE 000      > 340 MS
0690*               001
0691*               010
0692*               011
0693*
0694*               100      > 1 SEC
0695*               101      > 10SEC
0696*               110      > 100 SEC
0697*               111      > 1000 SEC
0698*
0699*
0700   00651 000000  WAIT  NOP
0701   00652 002400        CLA
0702   00653 070565        STA CNTR1      CLEAR CLOCK COUNTER
0703   00654 060507        LDA TCD
0704   00655 001323        RAR,RAR        CHECK FOR MINIMUM DELAY
0705   00656 000010        SLA            BIT 2 SET
0706   00657 024663        JMP WAIT1      YES, GO SCAN TIME CODE
0707   00660 003400        CCA            NO. SET MIN. DELAY.
0708   00661 070566        STA CNTR2      -1
0709   00662 024701        JMP WAIT3      GO TO CLOCK COUNTERS
0710*
0711*
0712   00663 060707  WAIT1 LDA WAIT5      SET UP SCANNER
0713   00664 070706        STA WAIT4
0714   00665 034706        ISZ WAIT4
0715   00666 060715        LDA TM2        GET STARTING CONSTANT.
0716   00667 070714        STA WAIT6      TO WORKING REGISTER.
0717   00670 060507        LDA TCD        GET TIME CODE.
0718   00671 010512         AND MSK1
0719   00672 050714  WAIT2 CPA WAIT6      IS THIS THE ONE?
0720   00673 024677        JMP *+4        YES, GO TO WAIT2
0721   00674 034714        ISZ WAIT6      INCREMENT WORKING TABLES.
0722   00675 034706        ISZ WAIT4      INCREMENT WORKING TABLES.
0723   00676 024672        JMP WAIT2      CHECK AGAIN
0724   00677 160706        LDA WAIT4,I    YES, GET CONSTANT
0725   00700 070566        STA CNTR2
0726*
0727*
0728   00701 034565  WAIT3 ISZ CNTR1      INCREMENT FIRST CLOCK COUNTER.
0729   00702 024701        JMP *-1
0730   00703 034566        ISZ CNTR2      INCREMENT SECOND CLOCK COUNTER.
0731   00704 024701        JMP WAIT3      LOOP AGAIN.
0732   00705 124651        JMP WAIT,I     EXIT.
0733*
0734*
0735*
0736   00706 000000  WAIT4 NOP
0737   00707 000707  WAIT5 DEF *
0738   00710 177775        DEC -3
0739   00711 177742        DEC -30
0740   00712 177324        DEC -300
0741   00713 172110        DEC -3000
```

```
0742*
0743   00714 000000  WAIT6 NOP             WORKING REGISTER.
0744   00715 000004  TM2   OCT 4           CONSTANT.
0745*
0746*
0747*
0748*
0749*
0750*                      PRINTER ROUTINE
0751*
0752*
0753   00716 000000  OT2    NOP
0754   00717 070733         STA TMP1
0755   00720 074734         STB TMP2
0756   00721 102501         LIA 01          CHECK SW FOR BIT 5
0757   00722 001727         ALF,ALF
0758   00723 001723         ALF,RAR
0759   00724 000010         SLA             BIT 5 SET?
0760   00725 124716         JMP OT2,I       YES, DO NOT PRINT
0761   00726 060735         LDA ML          NO, PRINT ERROR MESSAGE
0762   00727 114102         JSB 102B,I
0763   00730 060733         LDA TMP1
0764   00731 064734         LDB TMP2
0765   00732 124716         JMP OT2,I       EXIT ROUTINE
0766*
0767   00733 000000  TMP1   OCT 0
0768   00734 000000  TMP2   OCT 0
0769   00735 000002  ML     OCT 2
0770*
0771*
0772                        END
** NO ERRORS*
```

# THE TIME OF DAY CLOCK LIBRARY

Customers who have a Time Base Generator have continually requested a TIME OF DAY CLOCK ROUTINE for use outside the world of the 2018 Executive system. Herein is contained documentation for the BAILEY CLOCK ROUTINE.

Since this is a library subroutine, it should be loaded after the main program but before the Fortran/Algol Library.

The Sub-Program is called CLOCK and has entry points

SETUP
CLOCK
.CLOK
STCLK
RDCLK
DATIM
HALT

which may be called from the source Program.

To initialize the time of Day Clock, the user program must

```
CALL SETUP
```

or

```
JSB SETUP
DEF (RETURN ADDRESS)
```

When this instruction is executed the CLOCK Routine will print

```
ENTER TIME (HRS: MIN: SEC:)
```

and the operator will then enter the time of day plus a half

minute or so. The operator then types the keys CR, LF, and the computer will halt with

```
102077
```

in the T Register. When the operator presses the Run Button, the real time of day will be maintained by the CLOCK Entry Point (not callable from user Program).

After the clock has been initialized, real time of day may be read by means of a

```
CALL DATIM (IH, IM, IS)
```

or

```
JSB DATIM
DEF (RETURN ADDRESS)
DEF IH
DEF IM
DEF IS
.
.
.
```

The actual arguments are three integer variables to which the subroutine assigns values of the time in hours (0 to 23), minutes (0 to 59), and seconds (0 to 59). The clock is initially set by means of a CALL SETUP. The clock ceases to be incremented when a halt operation is executed.

If the HALT operation was a result of a call to the HALT subroutine, the clock is reset to zero. Its value will remain at zero until set through use of the SET TIME OF DAY switch.

If the halt was due to a PAUSE statement or pressing of the HALT button on the console, the time is unchanged. When program operation is resumed, the clock is incremented from the existing value.

The Bailey Clock Routine maintains an integer clock at entry point .CLOK (no callable by a user Program). It may be set or checked through the use of STCLK and RDCLK SUBROUTINES. A

```
CALL STCLK (N)
```

or

```
JSB STCLK
DEF (RETURN ADDRESS)
DEF N
.
.
.
```

sets the clock to zero and causes it to be incremented by one every (N*10) milliseconds. The N must be an integer constant (1-32, ≡ 767).

A

```
CALL RDCLK (M)
```

or

```
JSB RDCLK
DEF (RETURN ADDRESS)
DEF M
```

assigns the value of the clock to the integer variable M. The clock continues to be incremented at the most recently specified interval until reset by another call to STCLK.

The subroutine HALT is used to halt the computer. It is similar to the PAUSE statement in that it waits for the completion of all input/output operations before halting the computer. In addition, however, it clears the time of day clock and inhibits incrementation of the binary clock. No message is written on the Teleprinter when the halt occurs. The format of the call is:

```
CALL HALT
```

or

```
JSB HALT
DEF (RETURN ADDRESS)
```

If the HALT subroutine is used, the time of day clock remains set to zero (midnight) until reset through a CALL SET UP.

If the PAUSE statement is used, or if the HALT button on the computer console is pressed, the time of day clock is incremented when the program operation is restarted, but the time will be incorrect. Incrementation continues with the time when the halt occurred.

0001 ASMB,R,B,L,T

```
.IOC.  X 000001
.DIO.  X 000002
.IAR.  X 000003
.ENTR  X 000004
M1     R 000000
M2     R 000001
M3     R 000002
C1     R 000003
C2     R 000004
CMIN   R 000005
CHRS   R 000006
TIME   R 000007
CM24   R 000010
INIT   R 000011
COUNT  R 000012
CNTR   R 000013
TEMP   R 000014
ERR    R 000015
HRS    R 000042
MIN    R 000043
SEC    R 000044
RARG   R 000045
SARG   R 000046
CLK1   R 000047
MCLK   R 000050
RCLK   R 000051
ARPNT  R 000052
ARAY1  R 000053
ARAY2  R 000054
ARAY3  R 000055
.DTCL  R 000056
DTCH   R 000057
TFLG   R 000060
TI.1   R 000061
TI.2   R 000062
TEXT1  R 000063
SETUP  R 000103
.MPY   X 000005
TIMER  R 000151
I.0    R 000156
I.1    R 000157
I.2    R 000160
I.3    R 000167
T.0    R 000173
T.1    R 000174
T.2    R 000203
CLOCK  R 000204
STAT   R 000224
.CLOK  R 000232
C.1    R 000240
STCLK  R 000245
RDCLK  R 000261
DATIM  R 000267
.DLD   X 000006
.DIV   X 000007
D.1    R 000310
```

```
DRAIN  R 000316
ERROR  R 000317
REPET  R 000322
HALT   R 000334
H.1    R 000347
**  NO ERRORS*
```

```
0001                    ASMB,R,B,L,T
0002*                    BAILEY  TIME-OF DAY                    *
0003*      THIS IS THE CLOCK ROUTINE NECESSARY TO MAINTAIN*
0004*      THE TIME OF DAY                                *
0005*                                                     *
0006*                                                     *
0007*                                                     *
0008   00000                NAM CLOCK
0009                        ENT SETUP,CLOCK,.CLOK,RDCLK,STCLK,DATIM,HALT
0010*                                                                *
0011*      THE TIME OF DAY MAY BE SET THRU THE KEYBOARD INPUT *
0012*      BY CALLING SETUP FROM THE MAIN PROGRAM             *
0013*                                                         *
0014*      A TIMER MAY BE SET WITH A CALL STCLK(N) , WHERE N  *
0015*      IS A MULTIPLIER OF 10 MS TO DETERMINE THE TIME     *
0016*      INTERVAL.                                          *
0017*                                                         *
0018*      THE NUMBER OF (N*10 MS) INTERVALS ELAPSED MAY BE   *
0019*      READ WITH A CALL RDCLK(N)                          *
0020*                                                                 *
0021*      THE TIME OF DAY MAY BE READ WITH A CALL DATIM(IN,IM,IS) *
0022*                                                                 *
0023                        EXT .IOC.,.DIO.,.IAR,,.ENTR
0024*                    *
0025*      CONSTANTS     *
0026*                    *
0027   00000 037400  M1     OCT 37400
0028   00001 000377  M2     OCT 77
0029   00002 100000  M3     OCT 100000
0030   00003 021400  C1     OCT 21400
0031   00004 000003  C2     OCT 3
0032   00005 000074  CMIN   DEC 60
0033   00006 007020  CHRS   DEC 3600
0034   00007 177766  TIME   DEC -10
0035   00010 177750  CM24   DEC -24
0036   00011 000000  INIT   NOP
0037   00012 000000  COUNT  OCT 0
0038   00013 177770  CNTR   DEC -8
0039   00014 000000  TEMP   NOP
0040   00015 006412  ERR    OCT 6412,5012,5012
       00016 005012
       00017 005012
0041   00020 054517         ASC 18,YOU MUST TURN ON THE CLOCK , DUM-DUM
       00021 052440
       00022 046525
       00023 051524
       00024 020124
       00025 052522
       00026 047040
       00027 047516
       00030 020124
       00031 044105
       00032 020103
       00033 046117
       00034 041513
       00035 020054
       00036 020104
```

```
       00037 052515
       00040 026504
       00041 052515
0042   00042 000316R HRS    DEF DRAIN
0043   00043 000316R MIN    DEF DRAIN
0044   00044 000316R SEC    DEF DRAIN
0045   00045 000000  RARG   NOP
0046   00046 000000  SARG   NOP
0047   00047 000000  CLK1   NOP
0048   00050 000000  MCLK   NOP
0049   00051 000000  RCLK   NOP
0050   00052 000053R ARPNT  DEF ARAY1
0051   00053 000000  ARAY1  NOP
0052   00054 000000  ARAY2  NOP
0053   00055 000000  ARAY3  NOP
0054   00056 000000  .DTCL  NOP
0055   00057 000000  DTCH   NOP
0056   00060 000000  TFLG   NOP
0057   00061 000000  TI.1   NOP
0058   00062 000000  TI.2   NOP
0059   00063 006412  TEXT1  OCT 6412,5012,5012
       00064 005012
       00065 005012
0060   00066 042516         ASC 13,ENTER TIME (HRS: MIN: SEC)
       00067 052105
       00070 051040
       00071 052111
       00072 046505
       00073 020050
       00074 044122
       00075 051472
       00076 020115
       00077 044516
       00100 035040
       00101 051505
       00102 041451
0061*
0062*      SETUP IS USED TO ENTER THE TIME OF DAY AND TO TURN ON THE     *
0063*      TIME BASE GENERATOR . THE TBG IS SET TO INTERRUPT EVERY       *
0064*      10 MSEC AND CALLS CLOCK AND .CLOK                             *
0065*      REAL TIME IS KEPT AS LONG AS THE COMBINATION OF SCALE FACTOR  *
0066*      AND MULTIPLIER CAUSE A CALL TO CLOCK EACH 10 MSEC             *
0067*                                                                    *
0068   00103 000000  SETUP  NOP
0069   00104 016004X        JSB .ENTR     SET INDIRECT BIT FOR EXIT
0070   00105 000000         NOP
0071   00106 016001X        JSB .IOC.     WRITE "ENTER TIME (HRS: MIN: SEC:)
0072   00107 020002         OCT 20002     ON COMMENT OUT DEVICE
0073   00110 026106R        JMP *-2
0074   00111 000063R        DEF TEXT1
0075   00112 000020         DEC 16
0076   00113 016224R        JSB STAT
0077   00114 002404         CLA,INA       READ HRS. ,
0078   00115 006404         CLB,INB             MIN.,
0079   00116 016002X        JSB .DIO.             SEC.,
0080   00117 000000         OCT 0         IN FREE FIELD
0081   00120 000121R        DEF *+1       FORMAT
```

```
0082  00121 062004R          LDA C2
0083  00122 065052R          LDB ARPNT
0084  00123 016003X          JSB .IAR.
0085  00124 062054R          LDA ARAY2       CONVERT MIN. TO SEC.
0086  00125 016005X          MPY CMIN
      00126 000005R
0087  00127 072061R          STA TI.1
0088  00130 076062R          STB TI.2
0089  00131 062053R          LDA ARAY1       CONVERT HRS. TO SEC.
0090  00132 016005X          MPY CHRS
      00133 000006R
0091  00134 000040           CLE
0092  00135 042061R          ADA TI.1        ADD HRS. AND MIN.
0093  00136 002140           SEZ,CLE
0094  00137 006004           INB
0095  00140 046062R          ADB TI.2
0096  00141 042055R          ADA ARAY3       ADD ON SEC
0097  00142 002140           SEZ,CLE
0098  00143 006004           INB
0099  00144 072056R          STA .DTCL
0100  00145 076057R          STB DTCH
0101  00146 102077           HLT 77B
0102  00147 016151R          JSB TIMER
0103  00150 126103R          JMP SETUP,I
0104*                                                          *
0105*     TIMER INITIATES D.43 FOR A 10 MSEC INTERRUPT         *
0106*     INTERVAL                                             *
0107*                                                          *
0108  00151 000000  TIMER NOP
0109  00152 036060R        ISZ TFLG          SET TIMER FLAG
0110  00153 062011R        LDA INIT          HAS D.43 BEEN FOUND ?
0111  00154 002002         SZA
0112  00155 026173R        JMP T.0           YES
0113  00156 036011R I.0    ISZ INIT          NO
0114  00157 016001X I.1    JSB .IOC.         A STATUS CHECK RETURNS THE DEVIC
0115  00160 040007  I.2    OCT 40007         IN THE A REGISTER
0116  00161 012000R        AND M1            ISOLATE DEVICE TYPE BITS
0117  00162 022003R        XOR C1            IS THIS DEVICE D.43 ?
0118  00163 002003         SZA,RSS
0119  00164 026167R        JMP I.3           YES
0120  00165 036160R        ISZ I.2
0121  00166 026157R        JMP I.1           NO , TRY AGAIN
0122  00167 062160R I.3    LDA I.2
0123  00170 012001R        AND M2            ISOLATE UNIT REFERANCE NUMBER FR
0124  00171 032174R        IOR T.1           MERGE IT WITH T.1
0125  00172 072174R        STA T.1
0126  00173 016001X T.0    JSB .IOC.         INITIALIZE D.43
0127  00174 021100  T.1    OCT 21100
0128  00175 102010         HLT 10B           REJECT
0129  00176 000202R        DEF *+4
0130  00177 000002         DEC 2             BUFFER LENGTH
0131  00200 016224R        JSB STAT
0132  00201 126151R        JMP TIMER,I
0133  00202 000002         DEC 2             SCALE FACTOR
0134  00203 000012  T.2    DEC 10            MULTIPLIER.
0135*
0136*     CLOCK IS THE MAIN CLOCK INTERRUPT SERVICE ROUTINE
```

```
0137*                                                                  *
0138   00204 000000  CLOCK NOP
0139   00205 062204R       LDA CLOCK
0140   00206 032002R       IOR M3
0141   00207 072204R       STA CLOCK
0142   00210 062060R       LDA TFLG        IS DAYTIME CLOCK ON ?
0143   00211 002003        SZA,RSS
0144   00212 016151R       JSB TIMER       NO
0145   00213 036007R       ISZ TIME        IS THIS A ONE SECOND TICK ?
0146   00214 126204R       JMP CLOCK,I     NO
0147   00215 062203R       LDA T.2         YES
0148   00216 003004        CMA,INA
0149   00217 072007R       STA TIME        RESET TIME FOR NEXT 10 TICKS
0150   00220 036056R       ISZ .DTCL
0151   00221 002001        RSS
0152   00222 036057R       ISZ DTCH
0153   00223 126204R       JMP CLOCK,I
0154*                        *
0155*     STATUS CHECK       *
0156*                        *
0157   00224 000000  STAT    NOP
0158   00225 016001X       JSB .IOC.
0159   00226 040000        OCT 40000
0160   00227 002020        SSA
0161   00230 026225R       JMP *-3
0162   00231 126224R       JMP STAT,I
0163*                                                                  *
0164*     .CLOK IS THE SYSTEM CLOCK                                    *
0165*     CONTROL IS TRANSFERRED HERE AT EACH CLOCK INTERRUPT. THE     *
0166*     SUBROUTINES STCLK AND RDCLK ARE SERVICED HERE                *
0167*                                                                  *
0168   00232 000000  .CLOK NOP
0169   00233 062047R       LDA CLK1
0170   00234 002007        INA,SZA,RSS
0171   00235 026240R       JMP C.1
0172   00236 072047R       STA CLK1
0173   00237 126232R       JMP .CLOK,I
0174   00240 062050R C.1   LDA MCLK
0175   00241 072047R       STA CLK1
0176   00242 036051R       ISZ RCLK
0177   00243 000000        NOP
0178   00244 126232R       JMP .CLOK,I
0179*
0180*
0181*
0182*                                                                  *
0183*     STCLK SETS THE RATE AT WHICH THE PROGRAM CLOCK IS            *
0184*     UPDATED TO N TIMES THE BASIC CLOCK INTERVAL                  *
0185*     WHERE N = THE PARAMETER IN THE CALL TO STCLK                 *
0186*                                                                  *
0187   00245 000000  STCLK NOP
0188   00246 016004X       JSB .ENTR
0189   00247 000046R       DEF SARG
0190   00250 162046R       LDA SARG,I
0191   00251 003004        CMA,INA         CLOCK RATE TO COUNTER
0192   00252 072050R       STA MCLK
0193   00253 103100        CLF 0
```

```
0194  00254 072047R          STA CLK1      INITIALIZE COUNTDOWN
0195  00255 002400          CLA
0196  00256 072051R          STA RCLK      0 TO PROGRAM CLOCK
0197  00257 102100          STF 0         TURN ON INTERRUPT
0198  00260 126245R          JMP STCLK,I
0199*
0200*      RDCLK - THE VALUE OF THE PROGRAM CLOCK IS RETURNED
0201*              IN THE ARGRUMENT OF THE CALL
0202*
0203  00261 000000  RDCLK NOP
0204  00262 016004X          JSB .ENTR
0205  00263 000045R          DEF RARG
0206  00264 062051R          LDA RCLK
0207  00265 172045R          STA RARG,I
0208  00266 126261R          JMP RDCLK,I
0209*
0210*      DATIM IS THE ROUTINE WHICH CONVERTS THE SECONDS COUNT
0211*      TO HRS : MIN : SEC  AND RETURNS THE TIME OF
0212*      DAY TO THE CALLING PROGRAM.
0213*
0214  00267 000000  DATIM NOP
0215  00270 016004X          JSB .ENTR     SET INDIRECT BIT FOR EXIT
0216  00271 000042R          DEF HRS       TRANSFER ARGRUMENT ADDRESSES.
0217  00272 062060R          LDA TFLG      HAS CLOCK BEEN INITIALIZED ?
0218  00273 002003          SZA,RSS
0219  00274 026317R          JMP ERROR     NO '
0220  00275 016006X          DLD .DTCL      YES LOAD TIME IN SEC
      00276 000056R
0221  00277 016007X          DIV CHRS      DETERMINE HRS.
      00300 000006R
0222  00301 172042R          STA HRS,I
0223  00302 060001          LDA 1
0224  00303 006400          CLB
0225  00304 016007X          DIV CMIN      DETERMINE MINS.
      00305 000005R
0226  00306 172043R          STA MIN,I
0227  00307 176044R          STB SEC,I     DETERMINE SEC.
0228  00310 062010R D.1      LDA CM24
0229  00311 142042R          ADA HRS,I
0230  00312 002020          SSA           IS THE HOUR >24
0231  00313 126267R          JMP DATIM,I   NO
0232  00314 172042R          STA HRS,I     YES
0233  00315 026310R          JMP D.1
0234  00316 000000  DRAIN NOP
0235*
0236*      ERROR NOTIFIES OPERATOR THAT THE CLOCK HASN'T
0237*      BEEN SETUP
0238*
0239  00317 000000  ERROR NOP
0240  00320 000000          NOP
0241  00321 000000          NOP
0242  00322 002404  REPET CLA,INA
0243  00323 006400          CLB
0244  00324 016001X          JSB .IOC.
0245  00325 020002          OCT 20002
0246  00326 026324R          JMP *-2
0247  00327 000015R          DEF ERR
```

```
0248   00330 000025          DEC 21
0249   00331 016224R         JSB STAT
0250   00332 102066          HLT 66B
0251   00333 026322R         JMP REPET
0252*                                                                  *
0253*      HALT ROUTINE ALLOWS ALL I/O OPERATIONS TO CEASE            *
0254*      BEFORE HALTING THE COMPUTER IT CLEARS THE TIME OF          *
0255*      DAY CLOCK AND INHIBITS INCREMENTATION OF THE BINARY        *
0256*      UNTIL RESET BY A CALL TO SETUP.                            *
0257*                                                                 *
0258   00334 000000  HALT  NOP
0259   00335 016004X         JSB .ENTR
0260   00336 000000          NOP
0261   00337 016224R         JSB STAT
0262   00340 016001X         JSB .IOC.
0263   00341 000000          NOP
0264   00342 062052R         LDA ARPNT
0265   00343 072014R         STA TEMP
0266   00344 062012R         LDA COUNT
0267   00345 072013R         STA CNTR
0268   00346 002400          CLA
0269   00347 172014R H.1     STA TEMP,I
0270   00350 036014R         ISZ TEMP
0271   00351 036013R         ISZ CNTR
0272   00352 026347R         JMP H.1
0273   00353 102044          HLT 44B
0274   00354 126334R         JMP HALT,I
0275*
0276*
0277*      END OF CLOCK PROGRAM.
0278*
0279                          END
**  NO ERRORS*
```